DDR4, just another evolutionary step in memory interfaces?

Especially in the embedded world new designs are just switched from DDR2 to DDR3 interfaces. There are many nice features in DDR3 to simplify design effort. But even there are many new training features the overall concept of DDR3 is still quite evolutionary compared to DDR2. Now JEDEC released the new DDR4 specification. Are there bigger changes now for DDR4?
Of course there are some obvious changes: The datarate was increased to a max. of **3.2Gb/s** per pin, the **density per device was increased to 16Gb** and the Voltage went down to **1.2V** in order to reduce power.
Another feature to reduce Power is a newly added supply Voltage: **VPP (2.5V).** Internally the DDR3 DRAM had to pump up the external 1.5V in order to get the required wordline levels. With the reduced VDD voltage it got more inefficient to generate this Voltage internally in the DRAM.
One small improvement on DDR4 can be found in the “write leveling”. In DDR2 it was required to match the trace length of the complete Bus (e. g. 64bit), while in DDR3 the length matching could be done for a byte lane only. But DDR3 specified that the training feedback from the DRAM was given on the lowest databit only. Due to this feature it was not allowed to swizzle data bit 0 on DDR3 systems. The DDR4 spec now defines that this **Write Leveling feedback should be given on all data bits in parallel**.
New is also a feature called **“per DRAM Addressability”**. While in DDR3 it was only possible to configure all DRAMs on a Rank in parallel now it is possible to configure single DRAMs by qualifying configuration commands by DQ0. Don’t understand this feature wrong! This is not for reading out data of a single DRAM, but for configuring ODT and Vref levels per DRAM.
The mentioned Vref level programming/training is another new feature for DDR4. **The databus is terminated to VDDQ** (compared to a center tap termination for DDR3). But this means, that the Vref level will change based on drive strength and loading. Therefore VrefDQ is not any more supplied externally, but **VrefDQ is generated internally in the DRAM**. The termination on the Command/Address bus is still a center tap termination to midlevel, and therefore VrefCA is still externally provided.
The limit of DDR3 speed increase is the internal memory core architecture with 8bit Prefetch. The internal speed of the DRAMs did not increase too much over years, the increase in speed was achieved by increasing the Prefetch. Another increase of the prefetch to 16 bit would have delivered too much data per read. So **DDR4 changed to a Bank Group concept** with the known 8bit prefetch. But this means, that the Bank groups need to be accessed alternating in order to utilize the full datarate of the device.
The **Data Bit inversion (DBI)** is known already for GDDR5. Data are inverted based on the information of the DBI_n pin. This helps to avoid simultaneous switching of many Data bits (but is not available on x4 DRAMs).
The **Command/Address parity (CA Parity)** for CA and CRC for Write Data helps to ensure integrity. But this requires some additional latency e. g. to allow the DRAM to execute the parity check.
To improve **high density devices 3D stacking (in special with TSV) was considered** and ChipID pins C0 to C2 have been defined.
Another feature especially the embedded people have asked for a long time is a **boundary scan mode for DRAMs.** It is mandatory for x16 devices, but just optional for x4/x8 devices.
There are several other features, especially on power saving (see Table1). The step from DDR3 to DDR4 seems quite bigger than from DDR2 to DDR3, but it could be still called an

"evolutionary step". The future will show if there are enough improvements in order to get a fast transition from DDR3 to DDR4 as industry expects.

Author and contact information:
Hermann Ruckerbauer is founder of "**EKH – EyeKnowHow**" (www.EyeKnowHow.de). EKH provides training and consulting in special on memory interfaces. In addition to memory all kind of High Speed Digital interfaces like PCIe, SATA are part of consulting, simulation and measurement services from EyeKnowHow.

	X4	X8	X16
Write Leveling	X	X	X
Temperature Controlled Refresh	X	X	X
Low Power Auto Self Refresh	X	X	X
Fine Granularity Refresh	X	X	X
Multi Purpose Register	X	X	X
Data Mask		X	X
Data Bus inversion (DBI)		X	X
TDQS		X	
ZQ Calibration	X	X	X
DQ Vref Training	X	X	X
Per DRAM Addressability	X	X	
Mode Register Readout	X	X	X
CAL mode	X	X	X
Write CRC	X	X	X
CA Parity	X	X	X
Control Gear Down Mode	X	X	X
Maximum Power Down mode	X	X	
Boundary Scan Mode			X
Additive Latency	X	X	
3DS (stacking) support	X	X	

Table 1: DDR4 Features by organisation