EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

DRAM Standards

DDR2 vs. DDR3

Disclaimer

- The following document was generated by a short screening of old documents and current specifications.
- Not all of the „old“ data was checked to be still valid in the latest Specs
- Some things might have changed in the latest specs!
- Not all changes can be covered in such a document
  - Only main changes are listed

DRAM Specification
Evolution of DRAM Standards

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Comparison of Key Features

Key Feature	SDR	DDR1	DDR2	DDR3
Per Pin Data Rate	66 – 133 Mb/s	200 – 400 Mb/s	400 – 800 Mb/s	800 – 1600 Mb/s
Channel Band Width	0.53 – 1.06 GB/s	1.6 – 3.2 GB/s	3.2 – 6.4 GB/s	6.4 – 12.8 GB/s
Slots per Channel	4 ... 8	4 (6 ... 8)	3 (4)	2 (3)
Termination for Cmd/Addr/Clock Bus	None	Mother Board	Mother Board	DIMM
Termination for Data Bus	None	Mother Board and Memory Controller	SDRAM (ODT) and Memory Controller	SDRAM (Dynamic ODT) and Controller
Synchronization for Cmd/Addr/Clock Bus	Single Ended Clock	Differential Clock	Differential Clock	Differential Clock
Synchronization for Data Bus	Single Ended Clock	Single Ended Strobe	Single Ended and Differential Strobe	Differential Strobe

DDR3 Key Features
(differences to DDR2 in blue)

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- Single Supply Voltage: 1.5 V
  - Low Voltage DDR3 @ 1.35V
  - DDR2: 1.8V (LV 1.55V available too)
- Speeds 800 – 1600Mb/s
  - 1866 / 2133 Mb/s will be available too
  - DDR2: up to 800 (1066 available too)
- Densities up to 8Gb
  - Attention: 8Gb defined with 2k Page Size
  - DDR2: max. Density: 4Gb

DDR3 Key Features
(differences to DDR2 in blue)

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- 8-Bit Prefetch Architecture
  - Burst Length 8
  - Burst Chop 4 Modes
    - Fixed via Mode Register or
    - Selectable On-The-Fly
  - Only Read burst switch between Sequential and Interleaved
  - DDR2: native BL = 4 (4n Prefetch), BL can be programmed to 8, Read and Write burst changes for Sequ. vs. Interleave
- Page Size:
  - 1 KByte Page Size for x4 and x8
    - Attention: 8 Gbit is defined with 2KByte
  - 2 KByte Page Size for x16 components

DDR3 Key Features
(differences to DDR2 in blue)

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- TDQS support for mixed x4/x8 configurations
  - DDR2: RDQS feature
- Asynchronous Reset
  - Power up Sequence changed due to Reset
  - No Reset in DDR2
- Signaling:
  - Differential Clock
  - Bidirectional, Differential Strobes
  - Single ended CCA and DQ Signals
  - DDR2 allows single ended DQS as well

DDR3 Key Features
(differences to DDR2 in blue)

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- Latency:
  - Programmable CAS Latency (CL),
  - Programmable CAS Write Latency (CWL)
  - Additive Latency (AL)
  - DDR2: WL = RL – 1
  - Different Latency values DDR3 vs. DDR2
- Multi-Purpose Register (MPR)
  - Temperature sensor Readout
  - Read timing calibration
  - No MPR in DDR2

DDR3 Key Features
(differences to DDR2 in blue)

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- System Level Timing Calibration Support via Write Leveling and MPR Read Pattern
  - No Write Leveling on DDR2
- Speed binning definition
  - Different definition between DDR2 and DDR3
- Self Refresh
  - ASR (temp dependent) optional in DDR3
  - No ASR on DDR2

DDR3 Key Features
(differences to DDR2 in blue)

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- ODT (RZQ=240 Ohm):
  - DDR3: RZQ/2, RZQ/4, RZQ/6, RZQ/8, RZQ/12
  - DDR2 ODT: 50/75 and 150 Ohm
- ODT control features:
  - Dynamic and direct ODT Control
  - DDR2: direct ODT control only
- Output Driver (OCD) Calibration
  - ZQ based Calibration on DDR3 (ZQCL / ZQCS Command)
  - MR based Calibration on DDR2
- Drive Strength:
  - DDR3: RZQ/6, RZQ/7
  - DDR2: Full and Reduced Strength Driver

DDR3 Key Features
(differences to DDR2 in blue)

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- ODT tolerances:
  - Asymmetric tolerance definition for DDR3
  - Symmetric tolerance definition on DDR2
- Asynchronous ODT
  - Not sure if there was a change vs. DDR2 (maybe in the timings ...)
- Power-Down Modes
  - Precharge Power-Down with Slow and Fast Exit,
  - Active Power-Down
  - Change in Definition and Timings vs. DDR2

DDR3 Key Features (differences to DDR2 in blue)

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- Mode Register and SPD content
  - Quite some Changes to DDR2 due to all the different features and changes!
- IO Parasitics
  - Reduced IO parasitics on DDR3 vs. DDR2
- DDR3 standard CA Topology
  - Fly by end Terminated (e. g. on DIMM)
  - Requires enhanced timing calibration like write levelization and read timing calibration
  - DDR2: Hybrid T symmetric and „identical“ timings for all DRAMs on the bus

DDR3 Key Features (differences to DDR2 in blue)

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- Number of balls
  - All balls populated on DDR3
  - Increased number of balls on DDR3 vs. DDR2, some balls not populated
- Address mirror friendly Ballout
  - Ballout allows simple placement on top and bottom of PCB with some mirrored addresses (need controller support)
  - No Address mirroring possible on DDR2
- Quad die ODT functionality
  - Changed between DDR2 and DDR3
- No separate VDDL supply on DDR3
  - VDDL supply pads on DDR2

Memory Interface Implementation

Part 1

Agenda

1) DRAM Functionality

2) DRAM Specification

3) DDR3 Memory System Implementation

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Memory Interface Implementation

Part 2

Agenda

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1) Simulation and Data Evaluation

2) Layout

3) Measurement

Agenda

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- 1) Simulation and Data evaluation
  - Introduction: DDR3 System example
  - Simulation Setup
  - Time Domain Simulation
  - Data Eye evaluation
  - AC/DC based eye mask with t_{SH} derating
  - LeadIn Length effects
  - Timing Budget calculation
  - Power Integrity
  - Jitter / X-Talk / Skin Effekt
  - Rules of Thumb
- 2) Layout
- 3) Measurement