EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

DRAM Standards
DDR2 vs. DDR3 vs. DDR4

Disclaimer

- **The following document was generated by a quick screening of old documents and current specifications.**
- **Not all of the „old“ data was checked to be still valid in the latest Specs**
- **Some things might have changed in the latest specs!**
- **Not all changes can be covered in such a document**
  - Only main changes are listed

DRAM Specification
Evolution of DRAM Standards

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Comparison of Key Features

Key Feature	SDR	DDR1	DDR2	DDR3	DDR4
Per Pin Data Rate	66 – 133 Mb/s	200 – 400 Mb/s	400 – 1066 Mb/s	800 – 2133 Mb/s	1.6 – 3.2Gb/s
Channel Band Width	0.53 – 1.06 GB/s	1.6 – 3.2 GB/s	3.2 – 8.5 GB/s	6.4 – 17 GB/s	12.8 – 25.6GB/s
Slots per Channel	4 ... 8	4 (6 ... 8)	3 (4)	2 (3)	2
Termination for Cmd/Addr/Clock Bus	None	Mother Board	Mother Board Hybrid T CA bus	DIMM FlyBy CA bus	DIMM FlyBy CA bus
Termination for Data Bus	None	Mother Board and Memory Controller	SDRAM (ODT) and Memory Controller	SDRAM (Dynamic ODT) and Controller	SDRAM (Dynamic ODT) and Controller
Synchronization for Cmd, Addr, Clock Bus	Single Ended Clock	Differential Clock	Differential Clock	Differential Clock	Differential Clock
Synchronization for Data Bus	Single Ended Clock	Single Ended Strobe	Single Ended and Differential Strobe	Differential Strobe	Differential Strobe

Not too much changes from DDR3 to DDR4 ???

DDR4 Key Features

- **Dual Supply Voltage: VDD/VDDQ=1.2V and VPP=2.5V**
  - DDR3: Single 1.5V (Low Voltage: 1.35V)
  - DDR2: Single 1.8V (Low Voltage: 1.55V)
- **Speeds: 1.6 – 3.2Gb/s**
  - DDR3: 0.8 – 2.133 Gb/s
  - DDR2: 400 to 1066 Mb/s
- **Densities up to 16Gb**
  - DDR3: 8Gb Attention: 8Gb defined with 2k Page Size
  - DDR2: max. Density: 4Gb

DDR4 Architecture

- **DDR4:**
  - 8bit Prefetch per Bank Group with Burst Length 8
  - Burst Chop 4 Burst Chop 4 (On the Fly or Programmable)
  - Only Read burst switch between Sequential and Interleaved
- **DDR3:**
  - 8b Prefetch with Burst Length 8
  - Burst Chop 4 (On the Fly or Programmable)
  - Only Read burst switch between Sequential and Interleaved
- **DDR2:**
  - native BL = 4 (4n Prefetch),
  - BL can be programmed to 8,
  - Read and Write burst changes for Sequ. vs. Interleave

DDR4 Page Size

- **DDR4:**
  - 512 Byte Page size for x4
  - 1 KByte Page size for x8
  - 2 Kbyte Page size for x16
- **DDR3:**
  - 1 KByte Page Size for x4 and x8
    - Attention: 8 Gbit is defined with 2KByte
  - 2 KByte Page Size for x16 components
- **DDR2:**
  - 1 KByte Page Size for x4 and x8
  - 2 KByte Page Size for x16 components

DDR4 TDQS (RDQS)

- **DDR4**
  - TDQS for x8 only
- **DDR3**
  - TDQS support for mixed x4/x8 configurations
- **DDR2:**
  - RDQS feature

DDR4 Reset

- **DDR4 / DDR3:**
  - Asynchronous Reset
- **DDR2**
  - No Reset in DDR2

DDR4 Signaling

- **DDR4/DDR3 Signaling:**
  - Differential Clock
  - Bidirectional, Differential Strobes
  - Single ended CCA and DQ Signals
- **DDR2 Signaling**
  - Allows single ended DQS as well

DDR4 Signaling (Termination)

- **DDR4**
  - High level ODT termination for DQ
  - CTT midlevel on DIMM termination for CA
- **DDR3**
  - CTT midlevel ODT termination for DQ
  - CTT midlevel on DIMM termination for CA
- **DDR2**
  - CTT midlevel ODT termination for DQ
  - CTT midlevel on motherboard termination for CA

DDR4 Latency

- **DDR4**
  - Programmable CAS Latency (CL),
  - Programmable CAS Write Latency (CWL)
  - CS to CA Latency (CAL)
  - ODT Latency
  - CRC Latency
  - Parity Latency (PL)
- **DDR3**
  - Programmable CAS Latency (CL),
  - Programmable CAS Write Latency (CWL)
  - Additive Latency (AL)
- **DDR2**
  - WL = RL – 1

- **Different Latency values DDR4 vs. DDR3 vs. DDR2**

DDR4 MPRegister

- **DDR4**
  - 4 Programmable MPR registers with different pattern / readouts
- **DDR3**
  - Read timing calibration with 01 pattern
- **DDR2**
  - No MPR

Training Features

- **DDR4**
  - VrefDQ training
  - Write Leveling
  - Read calibration
- **DDR3**
  - Write Leveling
  - Read calibration
- **DDR2**
  - No specific support on DRAM for Trainings (DQS/DQ training can be done without DRAM support)

Self Refresh

- **DDR4**
  - Normal and extended Temperature controlled Refresh
  - Fine Granularity Refresh
  - LP ASR (low Power Auto Self Refresh)
  - No PASR (?)
- **DDR3**
  - ASR (temp dependent) optional in DDR3
  - PASR (Partial Array Self-Refresh) optional in DDR3
- **DDR2**
  - No specific support on DRAM for Trainings (DQS/DQ training can be done without DRAM support)

RTT

- **DDR4 (RZQ = 240 Ohm)**
  - RTT_NOM: RZQ / x (x=[1 to 7]
    - ➔ RTT: 34, 40, 48, 60,80,120, 240 Ohm
  - RTT_WR: RTT = RZQ/2 and RZQ/1
  - RTT_Park: RZQ / x (x=[1 to 7]
    - ➔ RTT: 34, 40, 48, 60,80,120, 240 Ohm
- **DDR3 (RZQ = 240 Ohm)**
  - RTT: RZQ / x (x=[2,4,6,8*,12*]
    - ➔ RTT: 40, 60, 120 Ohm (* only with restrictions)
  - RTT_WR: RTT = RZQ/4 and RZQ/2
- **DDR2 (no RZQ)**
  - 50 / 75 /150 Ohm RTT selectable

Output drive strength

- **DDR4 (RZQ = 240 Ohm)**
  - Ron: RZQ/7 and RZQ/5 Ohm
  - ZQ calibration of output drive Strength
- **DDR3**
  - Ron: RZQ/7 and RZQ/6 Ohm
  - ZQ calibration of output drive Strength
- **DDR2**
  - Full and Reduced Drive Strength
  - MR based calibration of output drive Strength