EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

Hunting PCIe Jitter

A real world example

Agenda

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1) Background and Motivation

2) Compliance Test Results

3) Eye diagram evaluation

4) SSC evaluation for TX and RefCLK

5) Follow back Data and Clock to signal sources

6) Verify Power Supply noise

7) Test Results with Fix and Conclusion

Background and Motivation

- **Compliance is tested on all kind of interfaces**
  - USB
  - SATA
  - Memory (more or less)
  - PCIe
- **Compliance tests are just resulting in “Pass” or “Fail”**
  - No additional information is given
- **In this case a standard PCIe Gen1 was failing and the root cause needed to be found**
- **Testequipment**
  - Agilent DSA91304 with 12 GHz probing system
  - Analysis Software
    - Agilent PCIe Compliance Test Suite
    - Agilent Jitter and Serial Eye test routines
  - PCIe Compliance board

Background and Motivation
Additional Information

- **Documents required:**
  - PCIe base Specification
  - CEM Specification
- **Additional information can be found in:**
  - Agilent PCI-Express Compliance Testing Methods of Implementation (Seventh edition, December 2010)
  - Agilent Jitter Seminar from 2006

Background and Motivation
Hardware Setup

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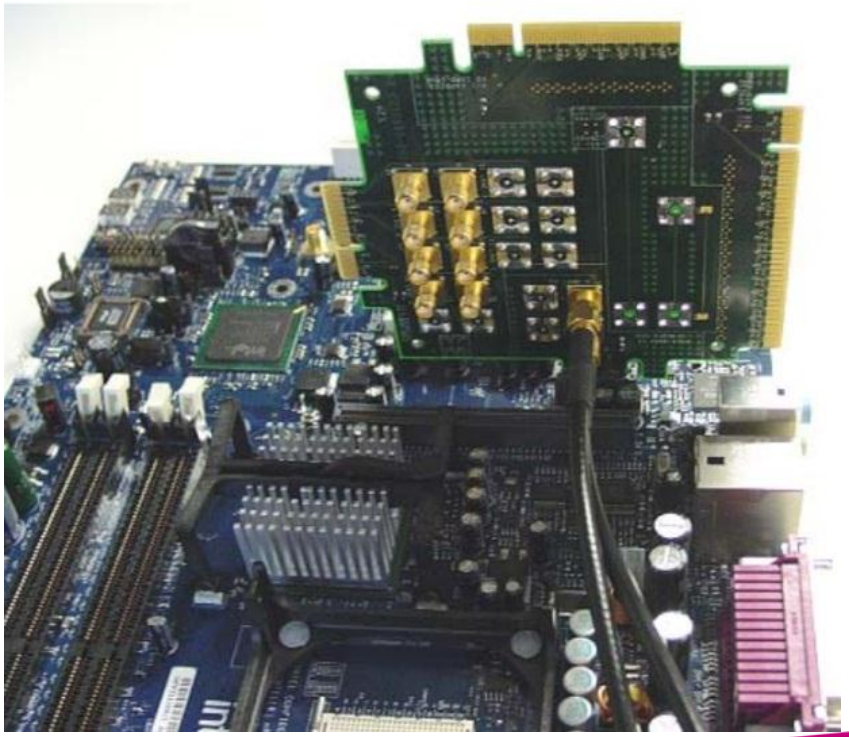
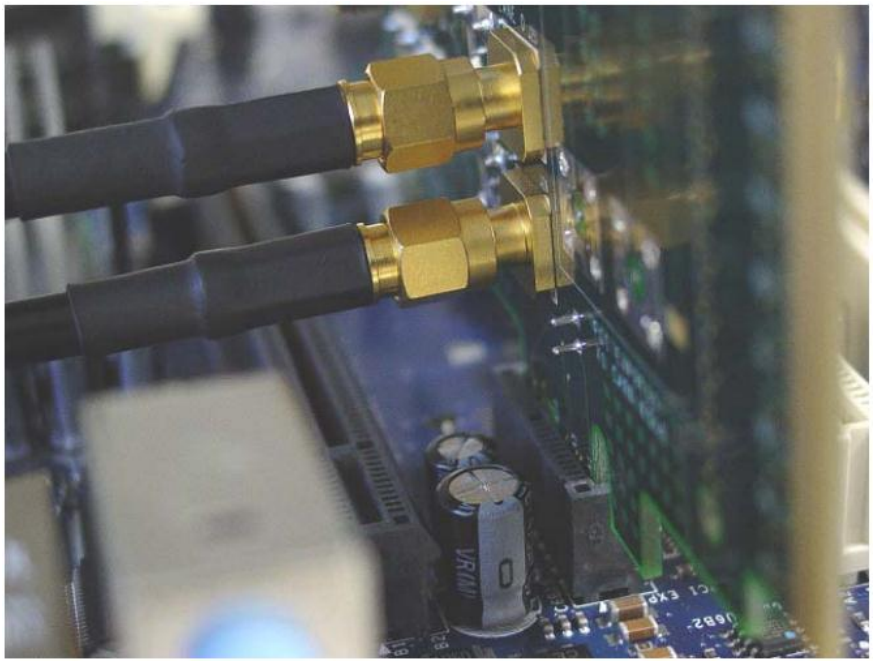
- Test Setup with compliance load board (PCIe1 CLB)
- Measurements done with direct connected SMA cables or 12 GHz differential Browser probe





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RefCLK
Compliance Test Result

- First the Reference clock was checked for spec compliance
- Nothing critical seen in the Refclk Compliance overview

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	Reference Clock, Phase Jitter (PCIE 1.1)	38.12ps	55.7 %	VALUE <= 86.00ps
✓	0	1	Reference Clock, Rising Edge Rate (PCIE 1.1)	1.62V/ns	30.0 %	600mV/ns <= VALUE <= 4.00V/ns
✓	0	1	Reference Clock, Falling Edge Rate (PCIE 1.1)	1.75V/ns	33.8 %	600mV/ns <= VALUE <= 4.00V/ns
✓	0	1	Reference Clock, Differential Input High Voltage (PCIE 1.1)	447mV	198.0 %	VALUE >= 150mV
✓	0	1	Reference Clock, Differential Input Low Voltage (PCIE 1.1)	-437mV	191.3 %	VALUE <= -150mV
✓	0	1	Reference Clock, Average Clock Period (PCIE 1.1)	21ppm	46.5 %	-300ppm <= VALUE <= 300ppm
✓	0	1	Reference Clock, Duty Cycle (PCIE 1.1)	50.8%	46.0 %	40.0% <= VALUE <= 60.0%

TX Compliance Test Results

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Directly Failing was only the UI test

- Sometimes the test was passing
- With some statistic also the Jitter or Eyewidth tests are failing

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✗	1	1	System Board Tx, Unit Interval (PCIE 1.1)	400.1650ps	**-18.8 %**	399.8800ps <= VALUE <= 400.1200ps
✓	0	1	System Board Tx, Template Tests (PCIE 1.1)	0.000	50.0 %	Zero Mask Failures
✓	0	1	System Board Tx, Median to Max Jitter (PCIE 1.1)	66.75ps	13.3 %	VALUE <= 77.00ps
✓	0	1	System Board Tx, Eye-Width (PCIE 1.1)	266.28ps	8.2 %	VALUE >= 246.00ps
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)	464.5mV	20.6 %	274.0mV <= VALUE <= 1.2000V
✓	0	1	System Board Tx, Peak Differential Output Voltage (NonTransition)(PCIE 1.1)	495.5mV	25.6 %	253.0mV <= VALUE <= 1.2000V

UI Specification from PCIe 1.1 Spec

- **Spec limits: 400ps +/- 300ppm = -/+ 0.120 ps**
  - For systems with SSC different limits apply

Table 116 UI from Table 4-5 of the Base Specification

Symbol	Parameter	Min	Nom	Max
UI	Unit Interval	399.88 ps	400ps	400.12 ps

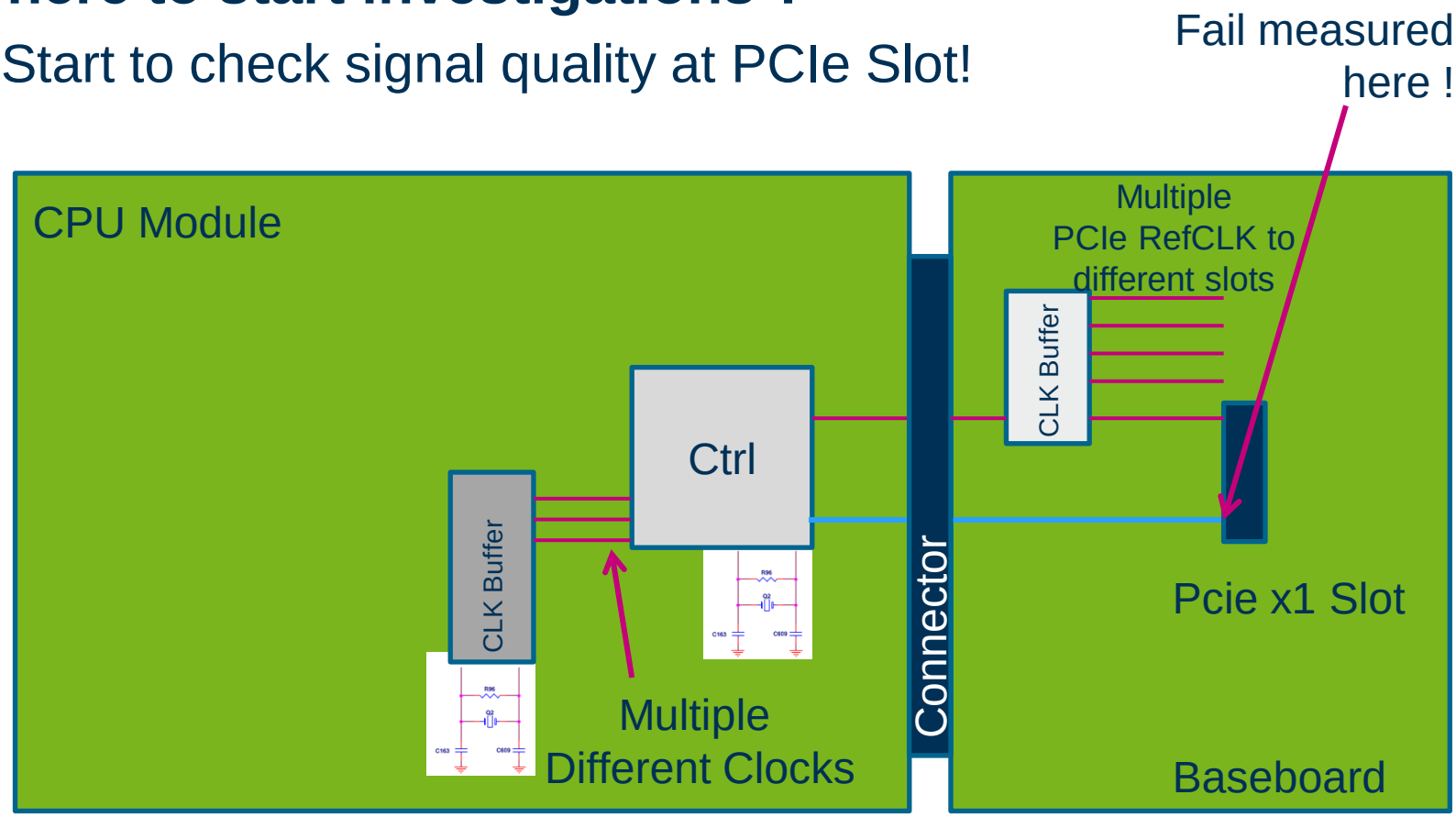
Test Definition Notes from the Specification

- UI (Unit Interval) is specified to be ±300 ppm.
- UI does not account for SSC dictated variations.

System Setup

Where to start investigations ?

- Start to check signal quality at PCIe Slot!



Compliance Test Results: Eye for Transition Bits

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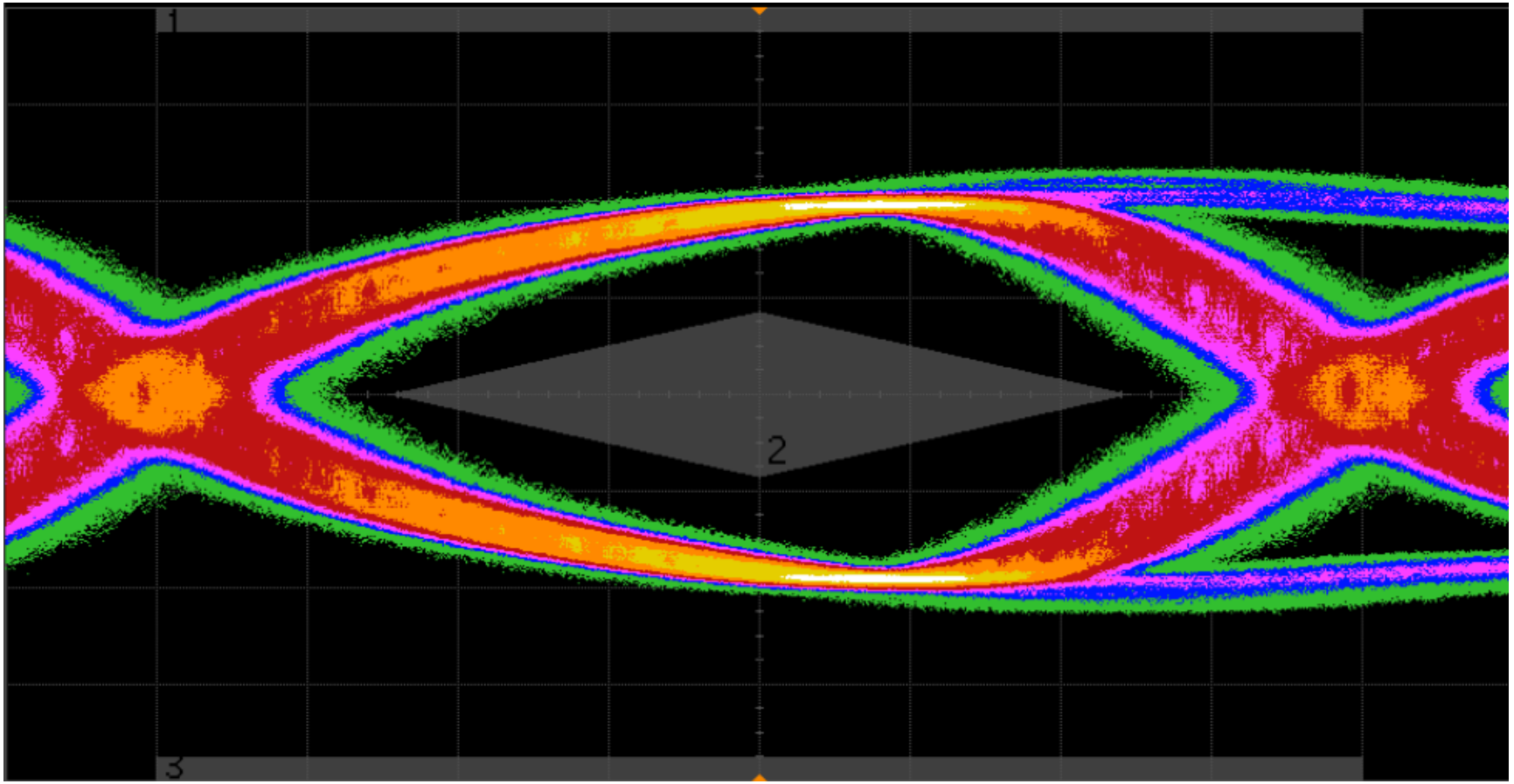
Eye diagram for Transition bits



Compliance Test Results: Eye for De-Emphasis Bits

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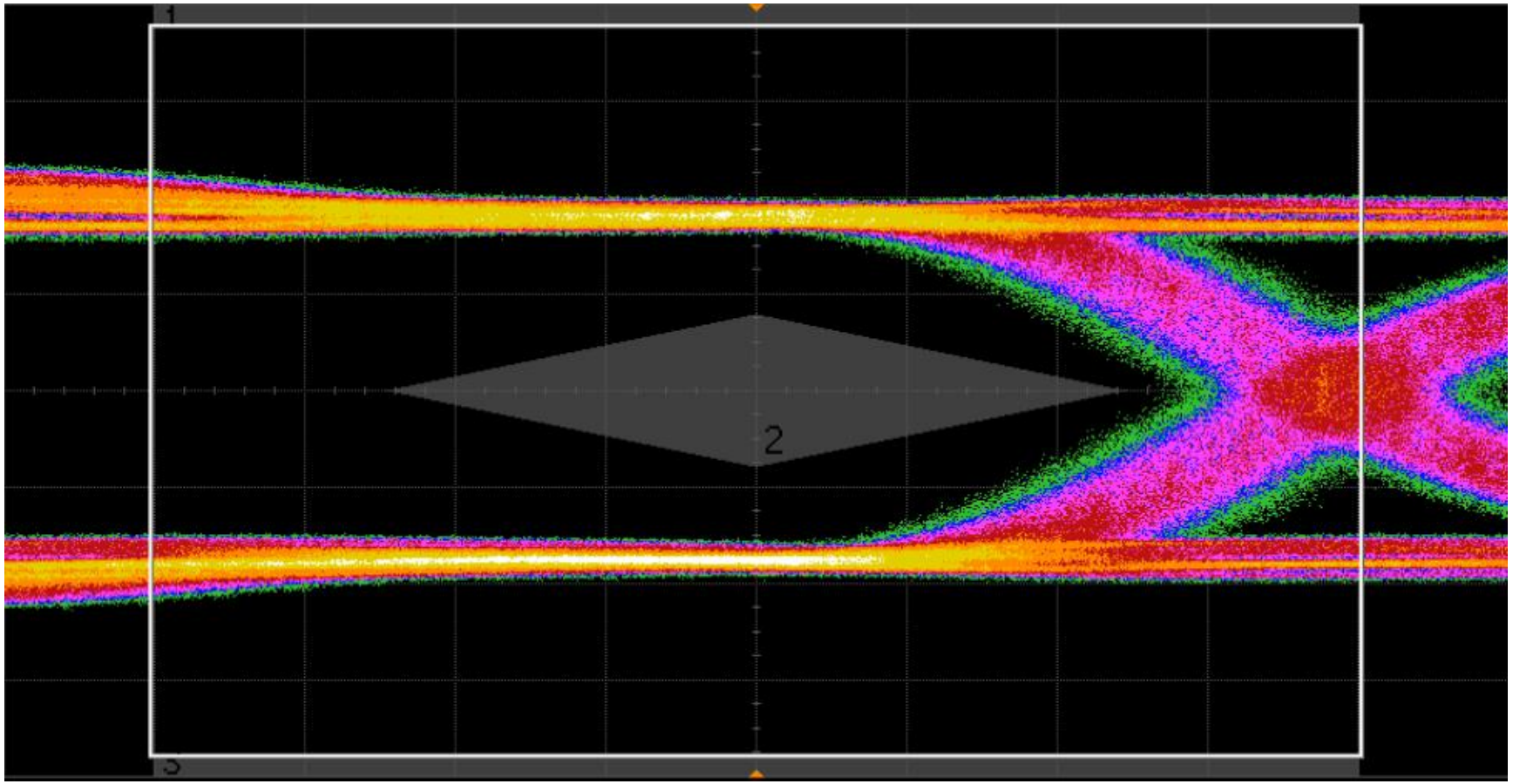
Eye Diagram non-Transition (De-Emphasis) bits



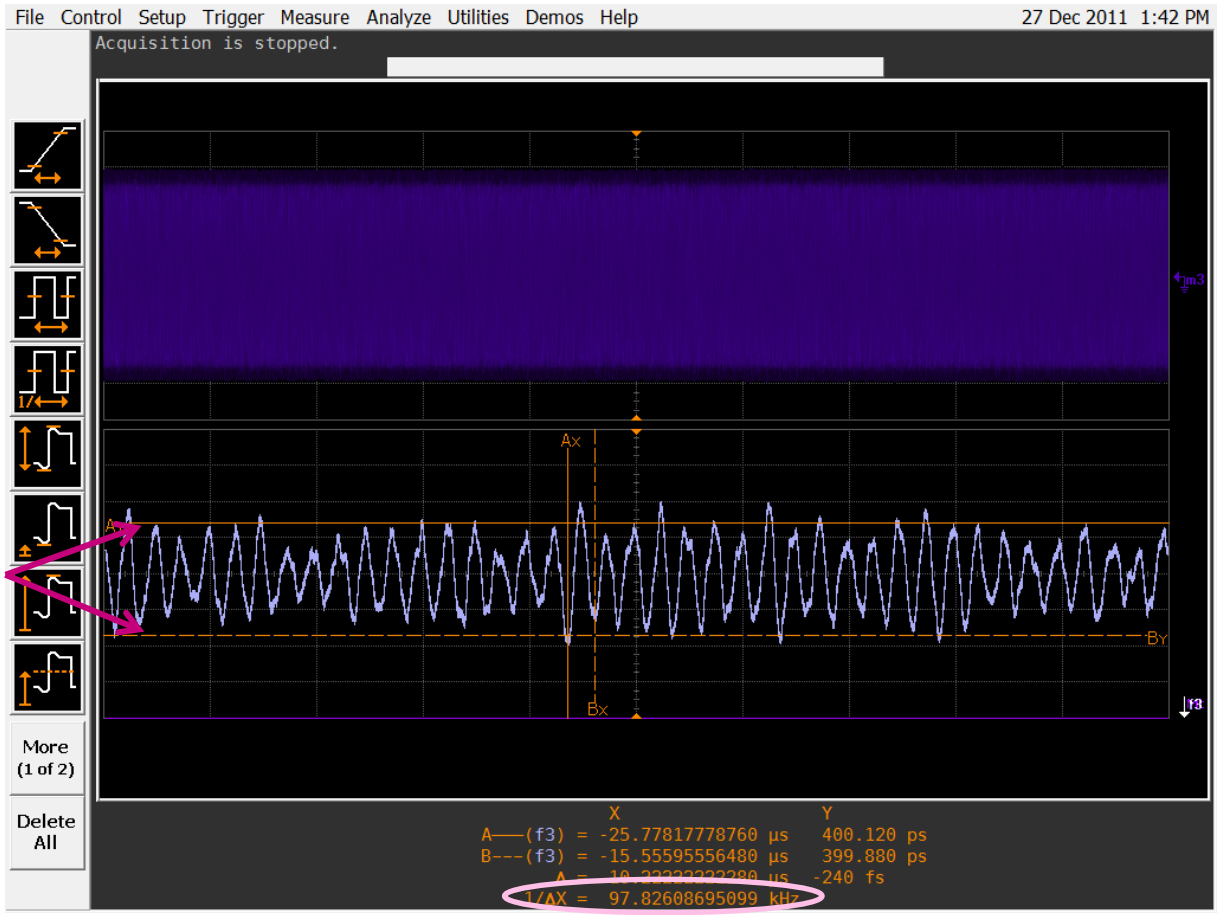
Eye diagram evaluation

- **Problem is not related to De-Emphasis settings as both eyes are similar bad**
  - In case the De-Emphasis Eye Jitter would be much worse as the Transition bit eye the De-Emphasis setting need to be optimized
- **Even the fail was marginal there was a big difference in eye quality to a reference system!**
  - So even if the test would have passed the difference should have been investigated!

Compliance Test Results
UI Time Trend

- The UI Time trend shows a “strange” modulation of the UI width.

Limits



Next investigations

- **Design and Layout Review of PCIe Signal routing did not show any hint on Problem**
  - Review is not part of this presentation
- **No additional debug possibilities in the Compliance test suite: We need to switch to other debug / analysis tools**
- **Starting point is the Eye Diagram with different settings**
  - One need to know the PCIe settings to correlate this Eye diagram to the Compliance test
  - PLL Bandwidth of 1.5MHz
    - Reduces sinusoidal Jitter -3dB at 1.5 MHz
    - The higher the Bandwidth the better the PLL can follow low frequency Jitter and generate a nice Eye diagram even for long traces including wander or SSC

Eye generated with manual Scope
Eye diagram features

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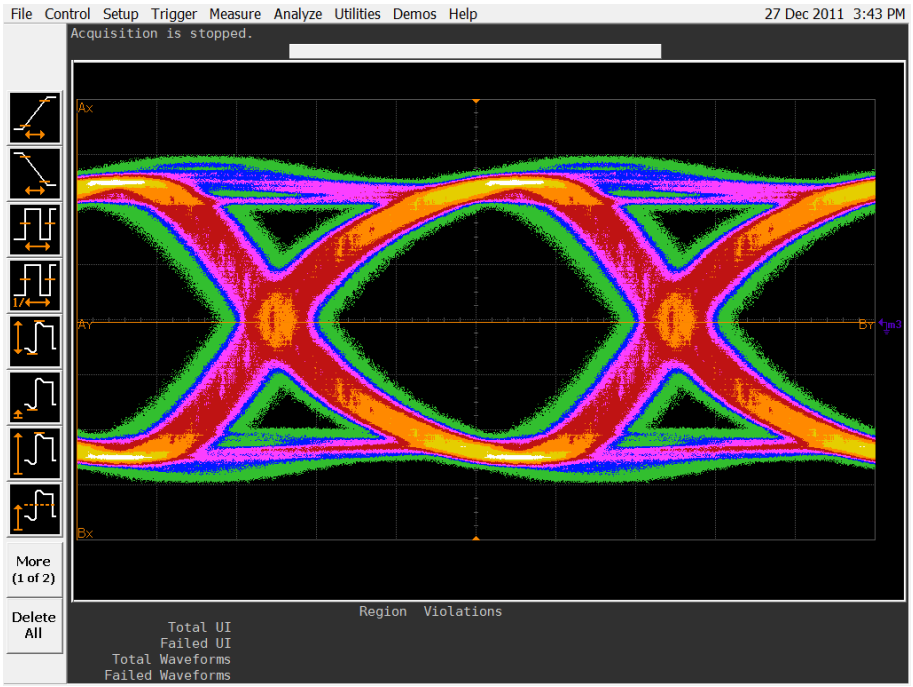
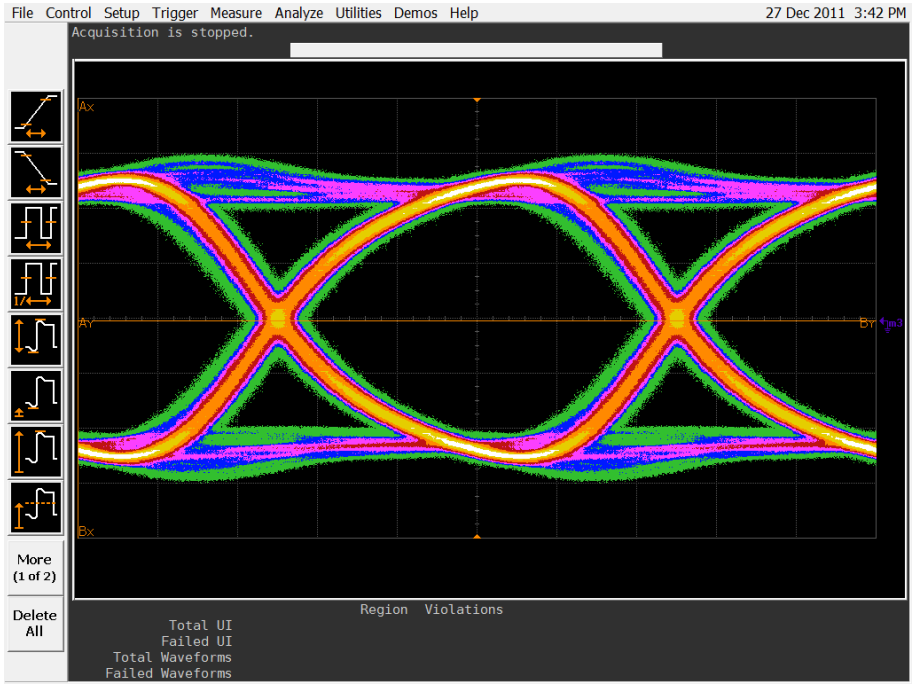
- **The additional filter in a 2nd order PLL would clean up the jitter**
  - If a system uses such a PLL for CDR it would not see this jitter
  - But in PCIe 1.1 such a 2nd order PLL is not required, but just mentioned as optional

1st order PLL



2nd order PLL

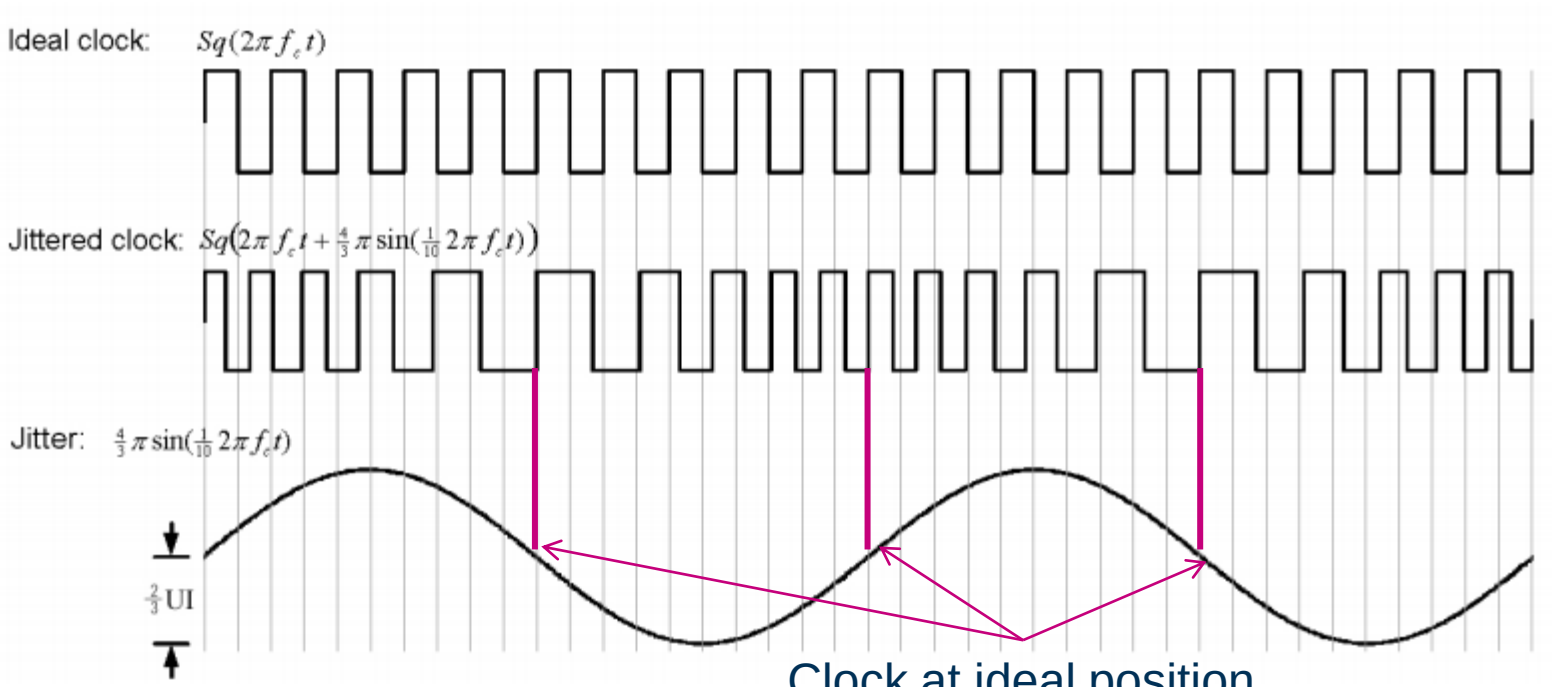


Some Jitter Basics

Jitter Explanation out of Agilent Jitter seminar 2006

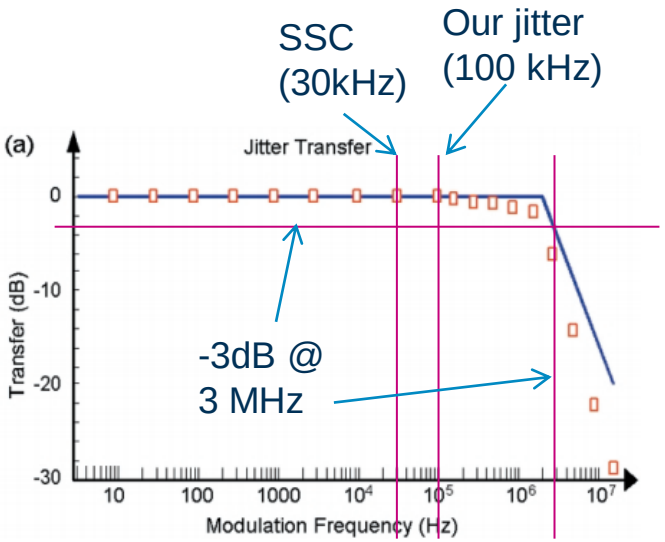
Jitter Analysis Techniques for High Data Rates (Application Note 1432)

Figure 1. Comparison of an ideal clock and a sinusoidally jittered clock. The jitter amplitude is ⅔ UI.

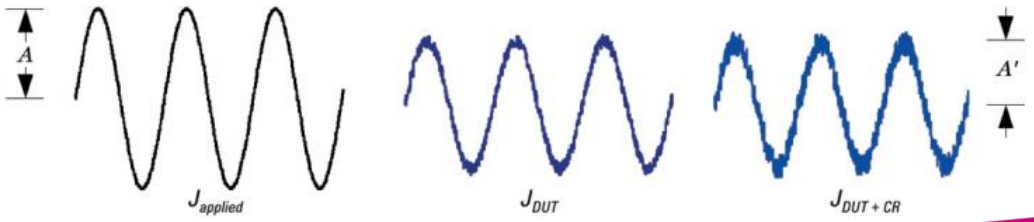


Some PLL Basics

- **PLL should follow Low Frequency Jitter (wander) and cancel High frequency Jitter**
- **Jitter Transfer function of a PLL**
  - Ideal behavior (blue line)
    - As long PLL follows low frequency Jitter in the eye this is not seen in the Eye Diagram
  - Possible real behavior (red Dots)
    - If the PLL/CDR can not follow this Jitter it will show up in the Eye Diagram
  - Things like Jitter peaking are not considered in this picture



- **Effect of CDR (and Jitter Transfer function) on Jitter**



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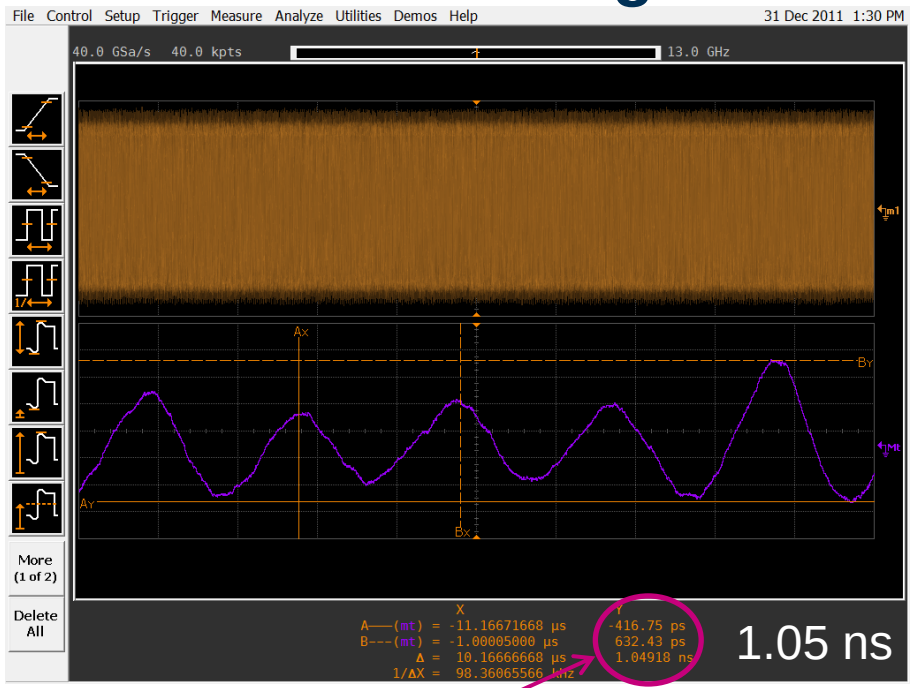
Evaluation of TX TIE with no PLL = Constant Clock

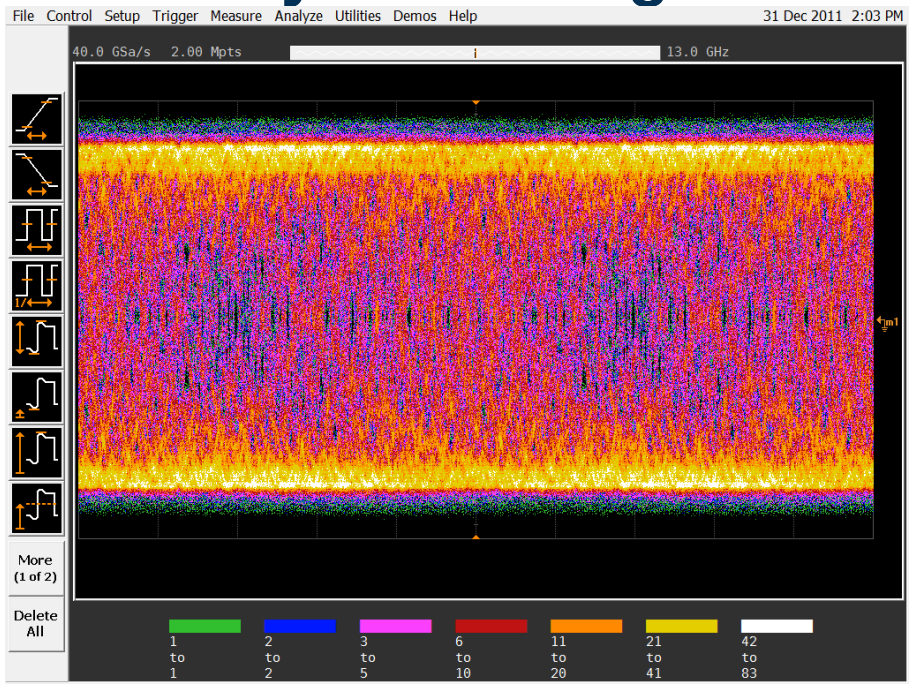
- **TIE = Time interval error**
  - Deviation of real clock edge from ideal clock edge position
- **Even the system is running without SSC there is no chance to generate a DataEye without a PLL**

TIE of TX signal



UI is 200ps!

Eye of TX signal



Evaluation of TX TIE with PLL BW = 1.5MHz

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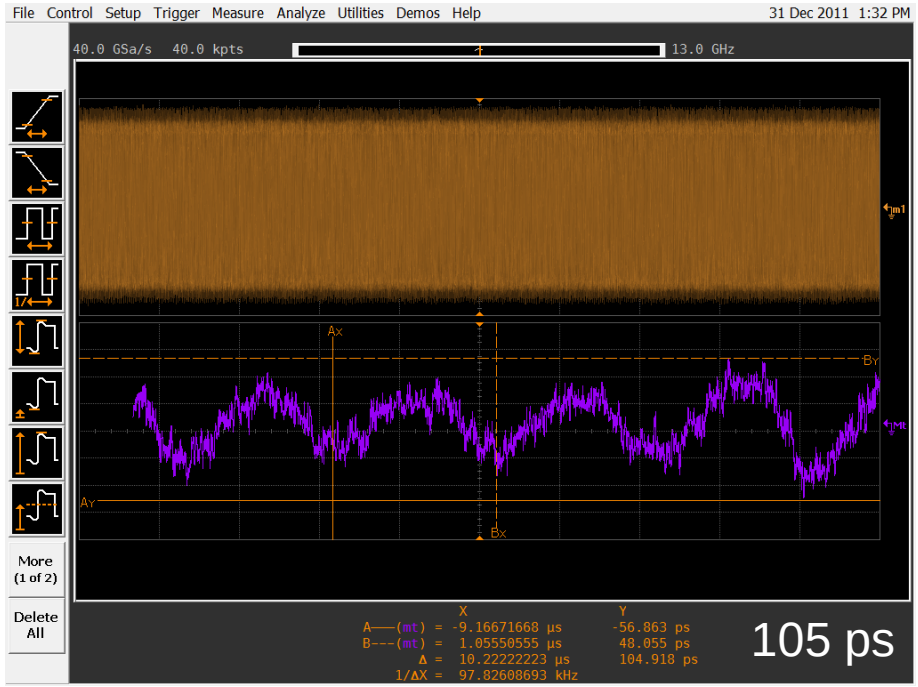
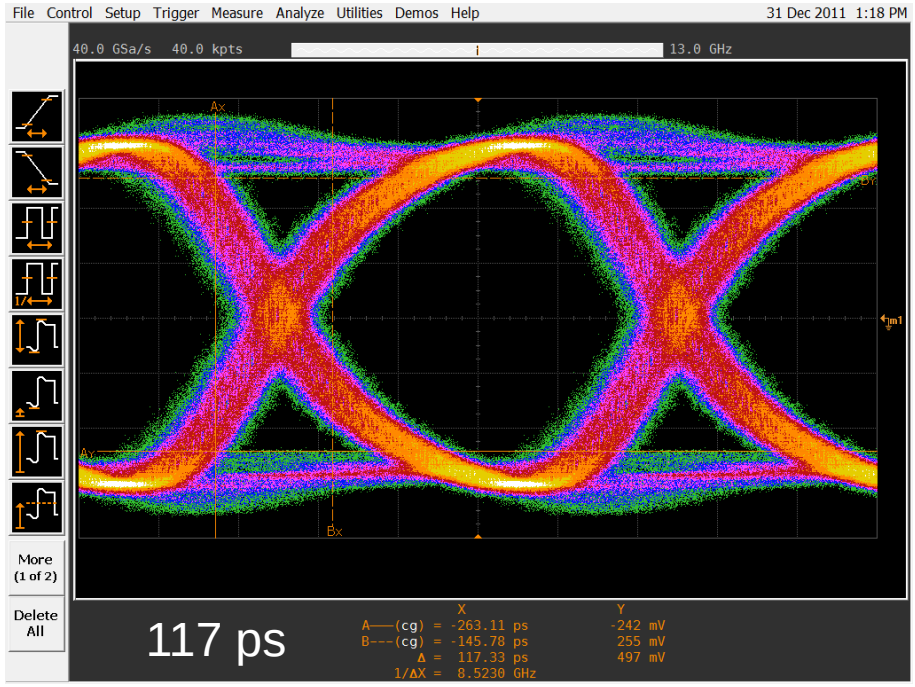
- With PLL BW = 1.5MHz an eye can be recovered, but with bad Jitter behavior!

TIE of TX signal



Eye of TX signal



Evaluation of TX TIE with PLL BW = 3MHz

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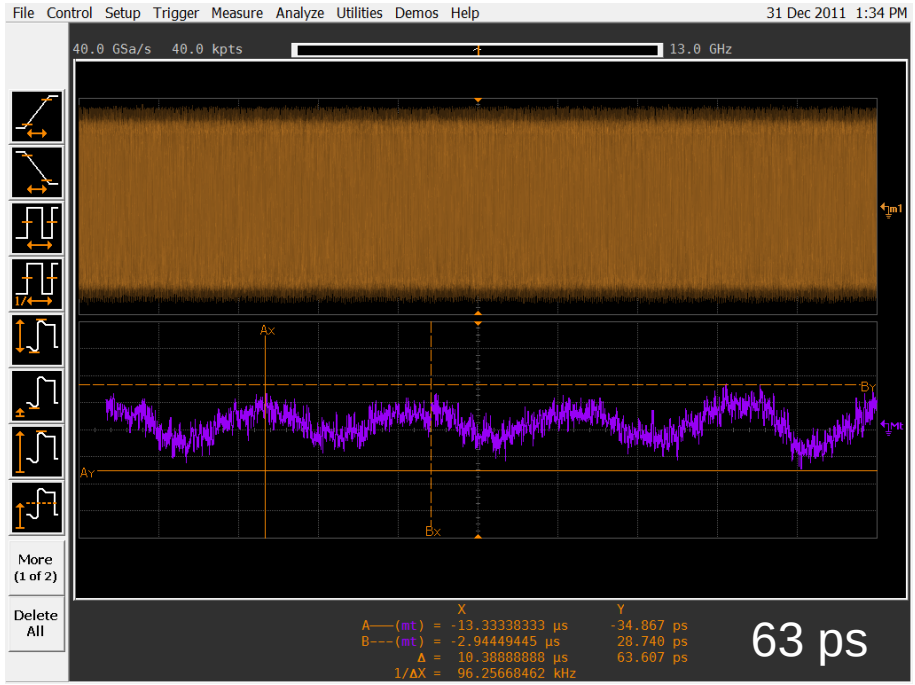
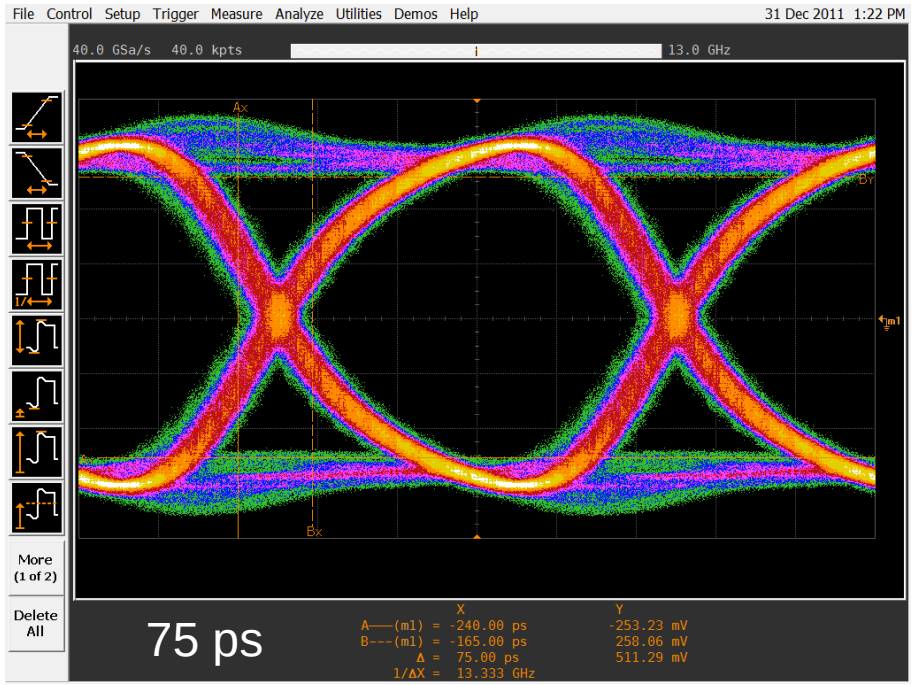
- With PLL BW = 3 MHz measured TIE Jitter gets smaller and Eye quality gets better!

TIE of TX signal



Eye of TX signal



Evaluation of TX TIE with PLL BW = 6MHz

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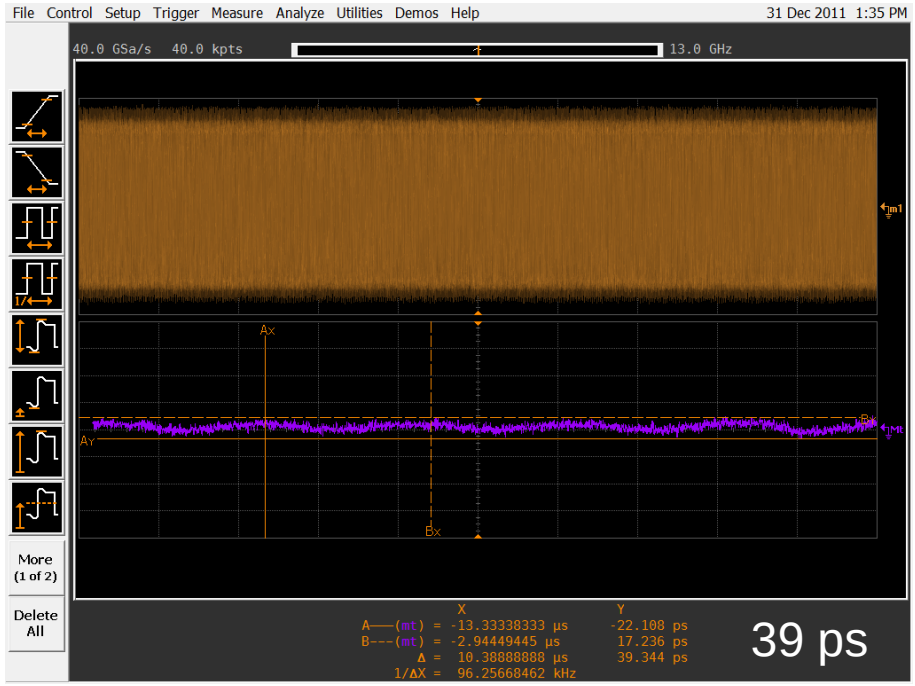
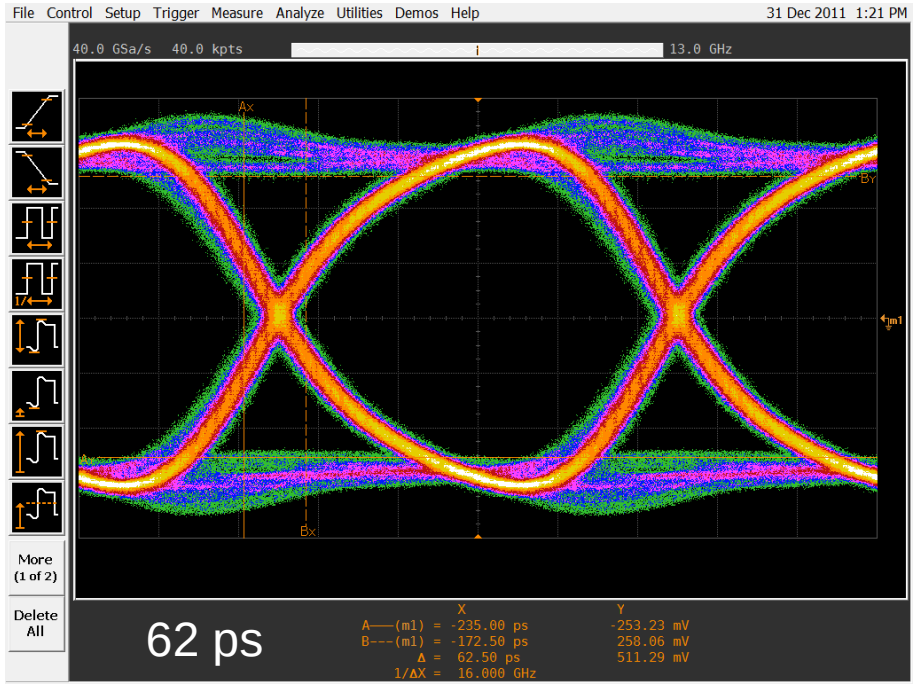
Further Improvement with PLL BW = 6 MHz

TIE of TX signal



Eye of TX signal



Evaluation of TX TIE with PLL 12MHz BW

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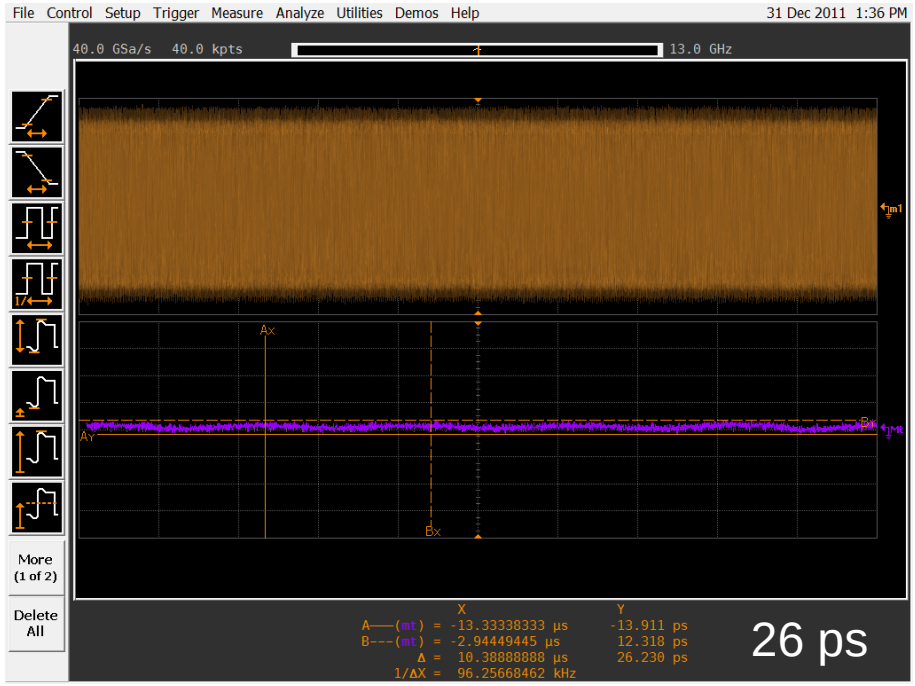
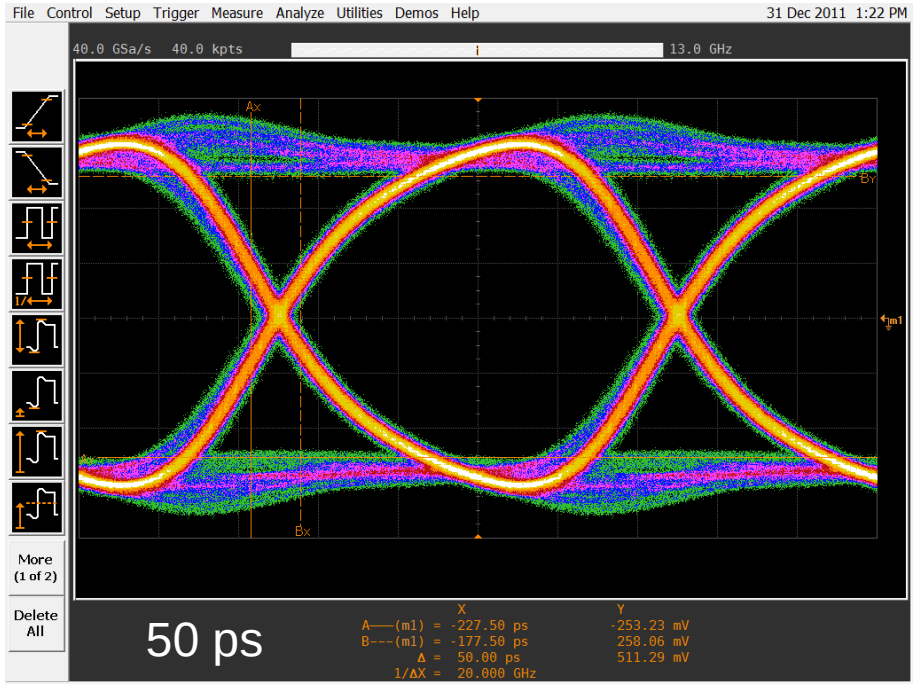
Further Improvement with PLL BW = 12 MHz

TIE of TX signal



Eye of TX signal



Conclusion

- **The higher the Bandwidth of the PLL the better the Measurement can track the “modulated” Jitter**
  - This improves the measured / calculated Eye diagram
- **To get a good eye the PLL would need follow the 100KHz modulation as good as possible**
  - With 1.5MHz BW setting the PLL seems to cancel some “Jitter”, that it would need to follow in order to generate a nice eye.
  - With higher BW the tracking ability is increased and the eye looks better

First guesses

- **What could cause this Modulation that is seen in the compliance test**
  - Introduced already on the CPU Module
    - Actively driven out by the Controller ?
    - Passive modulation due to coupling on the board ?
  - Introduced on the Baseboard ?
    - Not very likely, as this single CPU module type had problems, while others modules are working fine.
    - But this is not a solid argument, as an interaction between module and baseboard is often seen!

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RefCLK with SSC ON
"Strange" Histogram

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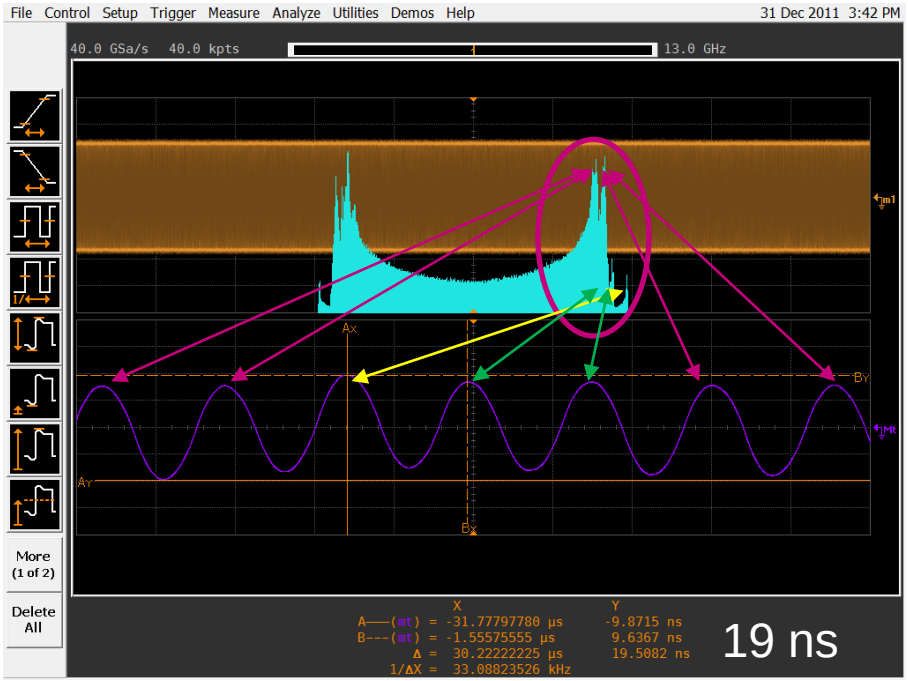
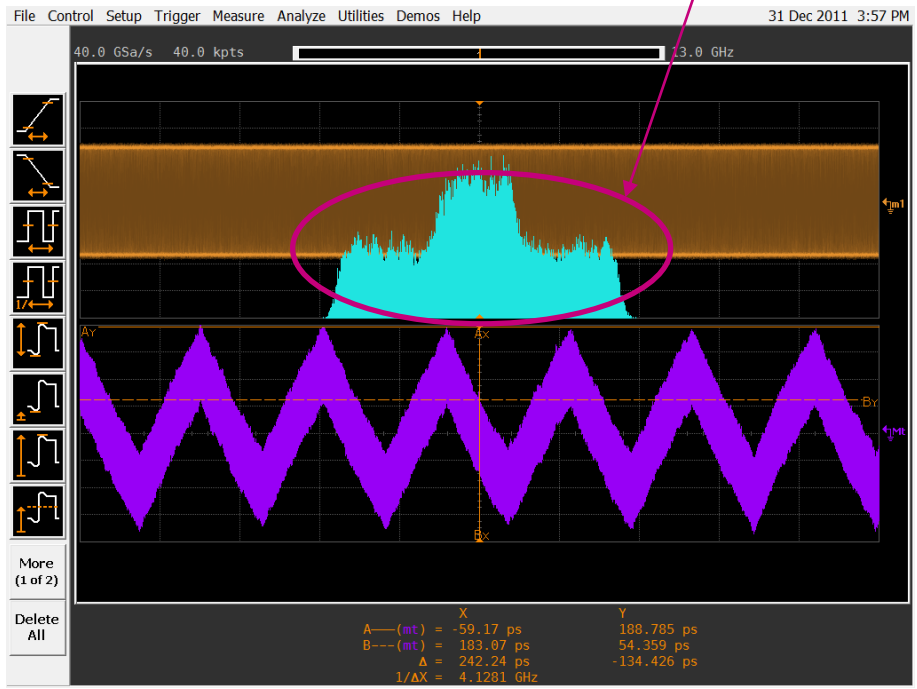
- TIE Jitter views on RefCLK with SSC
- Constant Clock
- PLL BW = 3MHz

?





RefCLK with SSC ON
“Strange” Histogram

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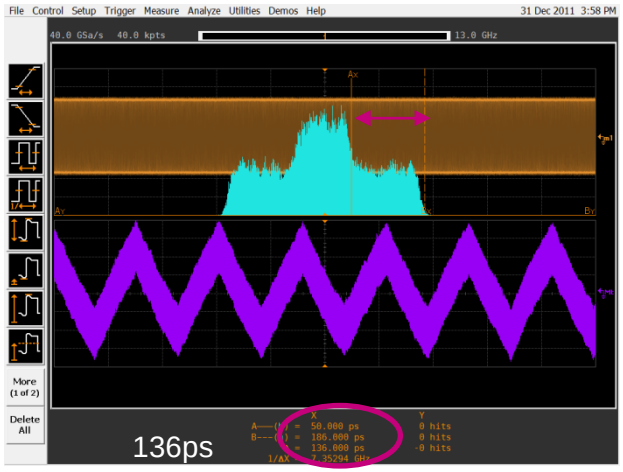
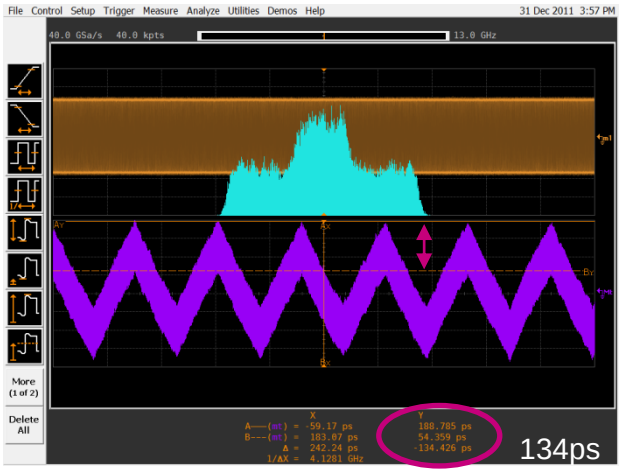
Measure on Histogram

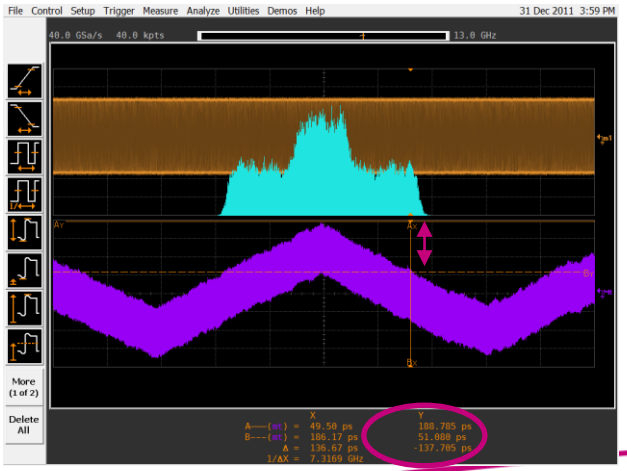


Measure on TIE

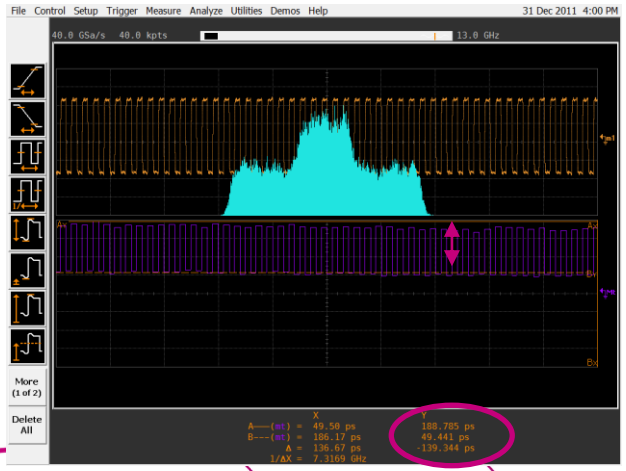


Just due to duty cycle and different crossing for rising / falling Edge …

Zoom1 on TIE



Zoom2 on TIE



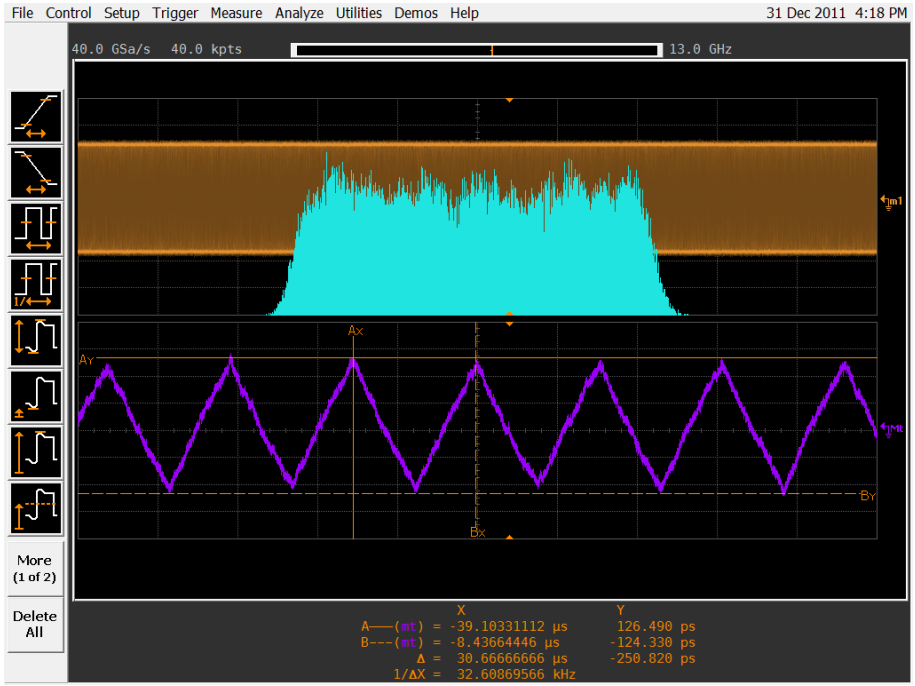
RefCLK with SSC ON "Strange" Histogram

- **Basically the measurement is correct, but:**
  - This effect had nothing to do with the real problem
  - This effect was hiding the real problem
- **Solutions to overcome this measurement artifact:**
  - Use "Smooth Data" results in "half Error" as it takes mean of Rising and Falling TIE result. This is only available for TIE, not for Histogram ➔ **Would be wrong and Does not help**
  - During Measurement definition one can select to use only Rising or Falling Edge. But this is only available for Clock TIE, not for Data TIE ➔ **Helps for Clocks, not for Data**
  - Adjust Thresholds manually in order to get a symmetric duty cycle ➔ **Best way to hide this effect**

One need to know very detailed what the measurement is doing an which options are available!

RefCLK with SSC ON
With Adjusted Thresholds

- This example should just show that it can be quite difficult to do correct measurements and interpret the results
- During this investigation several such Measurements have been taken and had to be interpreted.



Shifting the threshold by +80mV

Further Proceeding

- Check Clock and Data Signal Path
- Mainly use Constant Clock, as this gives a better indication of the problem as the PLL filtered clock

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RefCLK
Re-evaluate the RefClock result

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- The Compliance Test overview does not show anything noticeable

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	Reference Clock, Phase Jitter (PCIE 1.1)	38.12ps	55.7 %	VALUE <= 86.00ps
✓	0	1	Reference Clock, Rising Edge Rate (PCIE 1.1)	1.62V/ns	30.0 %	600mV/ns <= VALUE <= 4.00V/ns
✓	0	1	Reference Clock, Falling Edge Rate (PCIE 1.1)	1.75V/ns	33.8 %	600mV/ns <= VALUE <= 4.00V/ns
✓	0	1	Reference Clock, Differential Input High Voltage (PCIE 1.1)	447mV	198.0 %	VALUE >= 150mV
✓	0	1	Reference Clock, Differential Input Low Voltage (PCIE 1.1)	-437mV	191.3 %	VALUE <= -150mV
✓	0	1	Reference Clock, Average Clock Period (PCIE 1.1)	21ppm	46.5 %	-300ppm <= VALUE <= 300ppm
✓	0	1	Reference Clock, Duty Cycle (PCIE 1.1)	50.8%	46.0 %	40.0% <= VALUE <= 60.0%

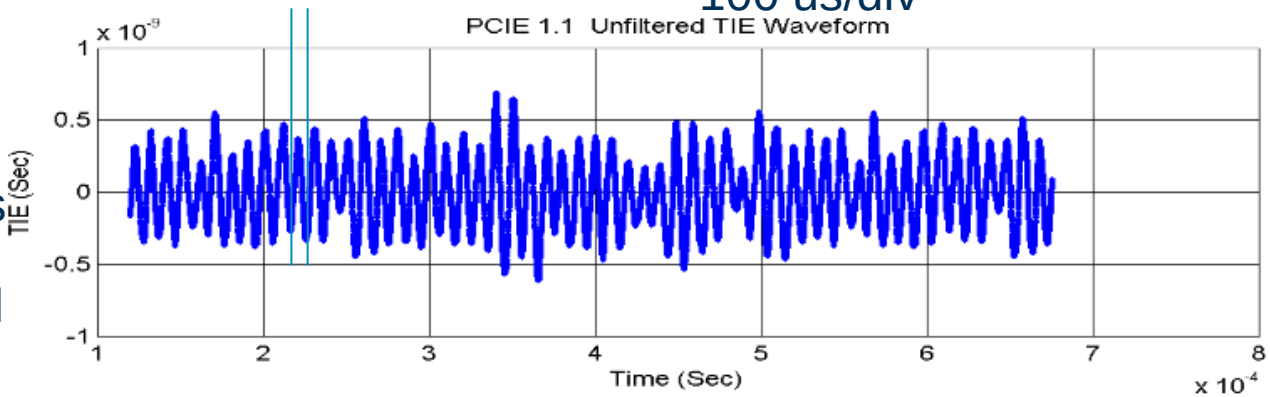
RefCLK Tie Jitter Test
SSC OFF

- **On the TIE jitter Time Trend we see again the 100KHz "Modulation"**

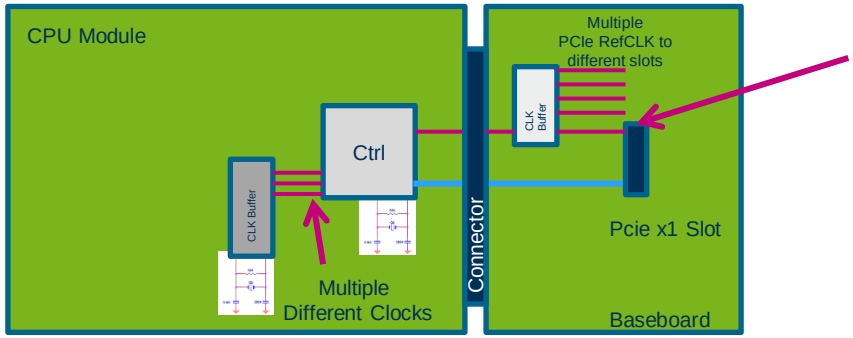
10us = 100KHz

100 us/div

+-1000 ps



This is the RefCLK Signal on the CLB



Measurement Point

TIE RefCLK on CLB 100MHz (tCK = 10ns)

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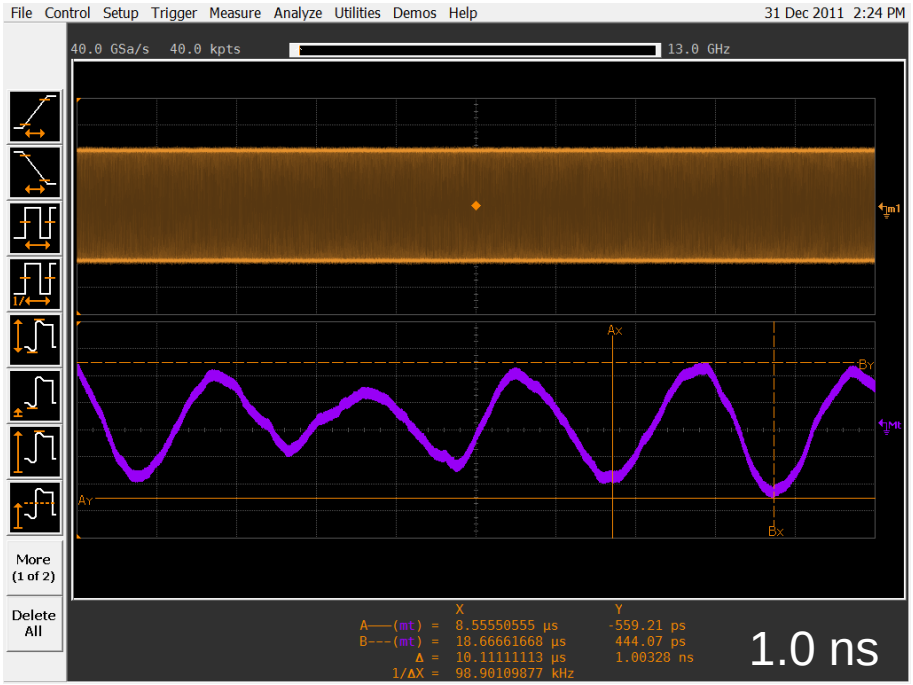
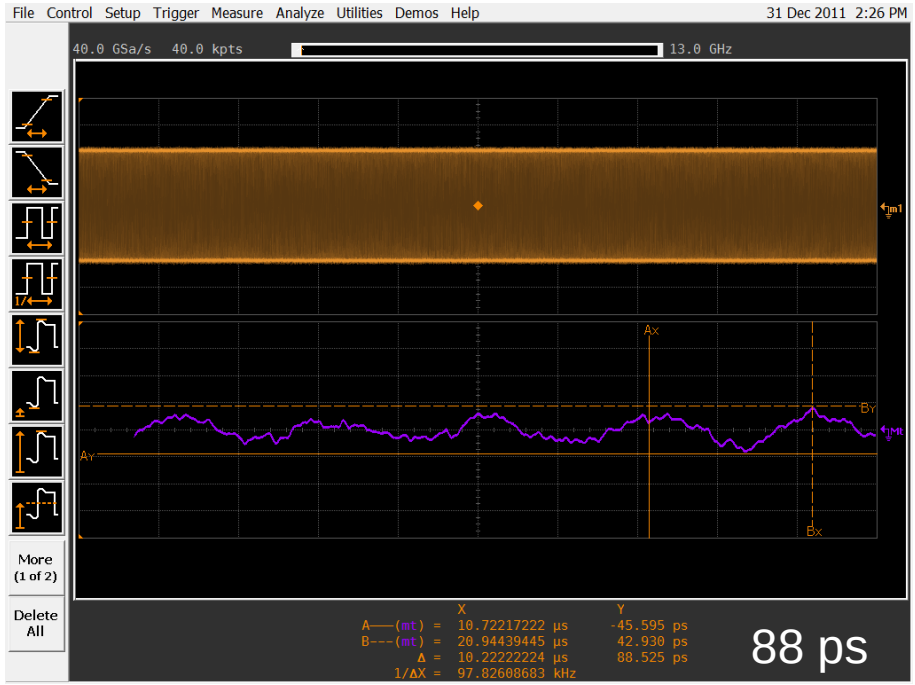
Success: 100KHz Jitter also found on RefCLK!

- Filtered: 88ps Error on a Clock with 10ns tCK

Constant Clock



PLL BW = 1.5MHz



BaseBoard RefCLK In Compliance Test

- **As the RefClock is re-driven by a clock buffer on the base board the input clock to this buffer was checked.**
  - No noticeable Results in the compliance test

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	Reference Clock, Phase Jitter (PCIE 1.1)	40.82ps	52.5 %	VALUE <= 86.00ps
✓	0	1	Reference Clock, Rising Edge Rate (PCIE 1.1)	2.06V/ns	42.9 %	600mV/ns <= VALUE <= 4.00V/ns
✓	0	1	Reference Clock, Falling Edge Rate (PCIE 1.1)	1.93V/ns	39.1 %	600mV/ns <= VALUE <= 4.00V/ns
✓	0	1	Reference Clock, Differential Input High Voltage (PCIE 1.1)	1.423V	848.7 %	VALUE >= 150mV
✓	0	1	Reference Clock, Differential Input Low Voltage (PCIE 1.1)	-1.396V	830.7 %	VALUE <= -150mV
✓	0	1	Reference Clock, Average Clock Period (PCIE 1.1)	16ppm	47.3 %	-300ppm <= VALUE <= 300ppm
✓	0	1	Reference Clock, Duty Cycle (PCIE 1.1)	49.3%	46.5 %	40.0% <= VALUE <= 60.0%

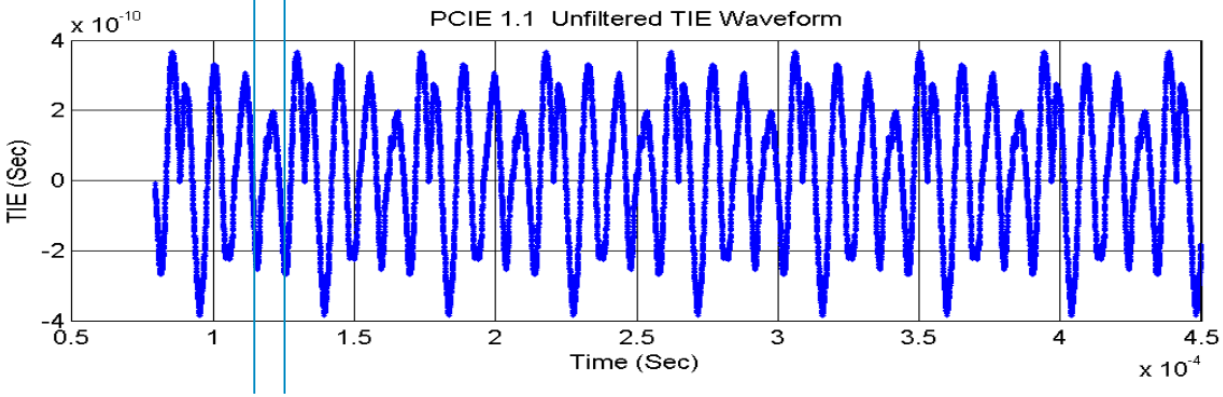
BaseBoard RefCLK In Compliance Test

- **Already the input to the Clock buffer shows the 100 KHz "modulation"**

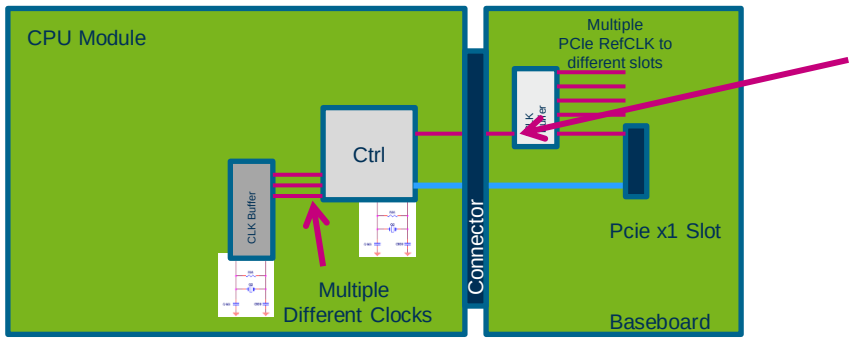
10us = 100KHz

50 us/div

+-400 ps



This is the RefCLK Signal Input on the Baseboard



Measurement Point

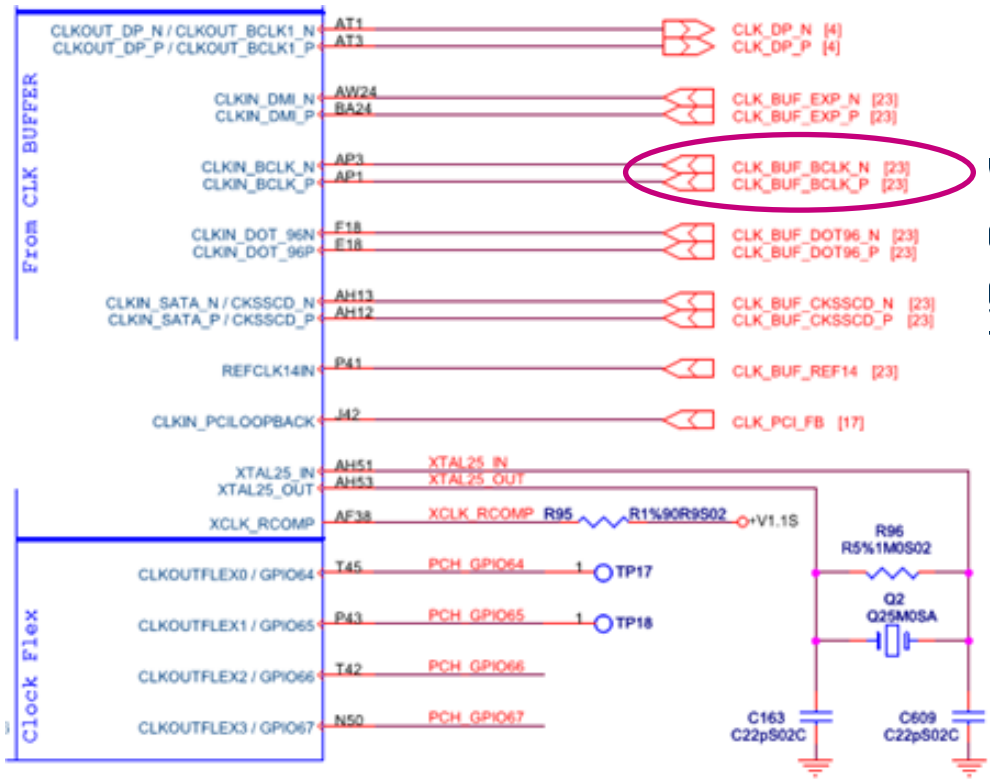
Status

- **TX Compliance test fail in UI width**
- **Jitter with ~ 100KHz Modulation seen on PCIe TX**
  - 100KHz is 3x Faster than SSC modulation with 33KHZ, therefore normal PLL will not follow this Jitter fast enough
- **Same modulation seen on CLB and Baseboard RefCLK**
  - Difficult to judge if this would cancel the Jitter. This Clock will be multiplied in TX/RX devices .. What happens to this modulation ?!?
- **Jitter is already on Signal driven out from the controller**
  - Check Clock / Data path back to find root cause

Root cause search

Which clock is used to generate PCIe signals ?

- Controller documentation regarding internal Clocking was really bad



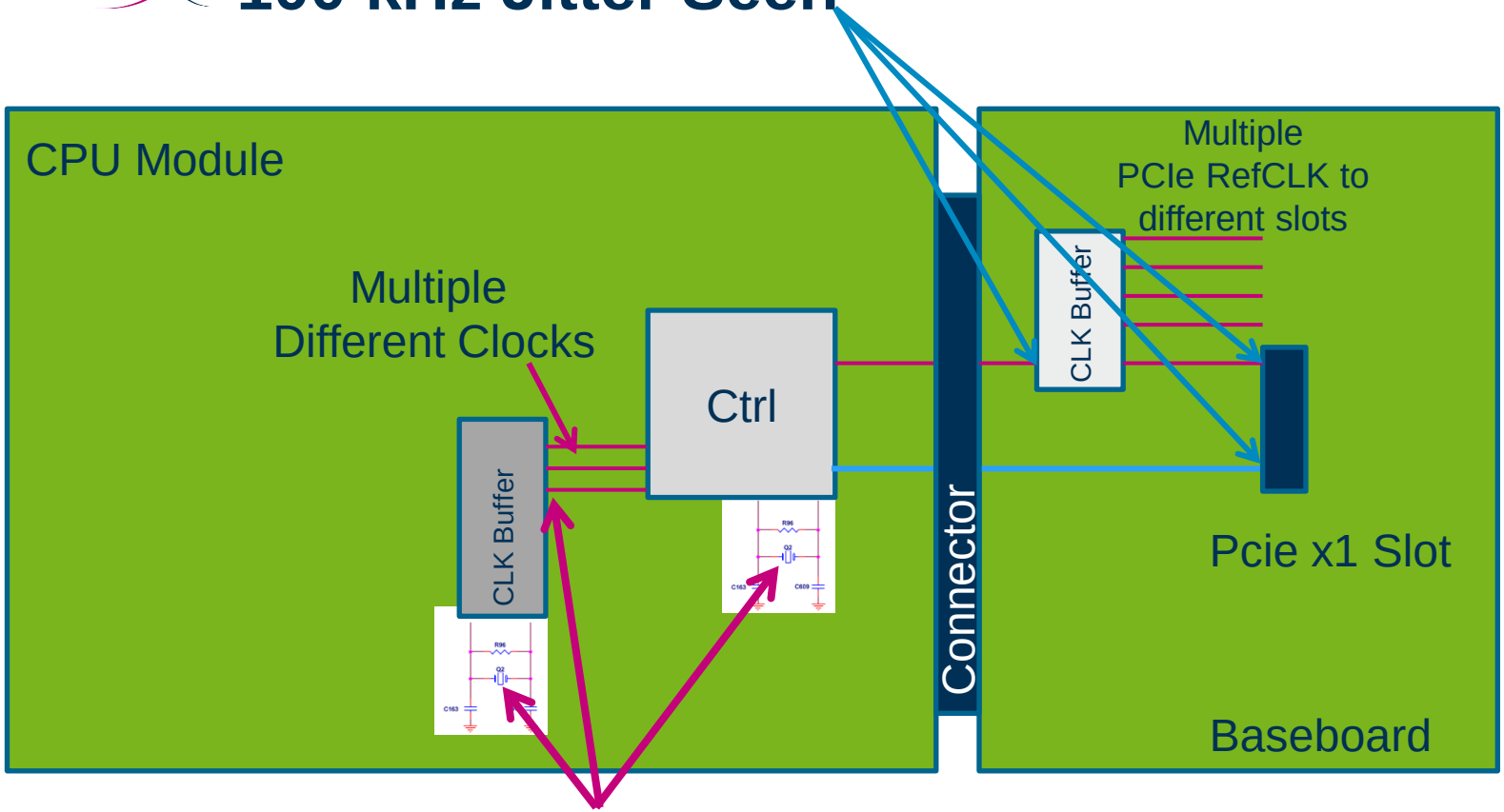
Controller

Which one of these input clocks from ICS Clock generator is used for PCIE TX Signals ?

Check Crystal performance ?

System Setup

100 kHz Jitter Seen



Possible Jitter Sources

ICS Clock Generator ICS9LPR501

- **ICS9LPR501 provides Clocks for the Controller**
  - ICS9LPR501 follows Intel CK505 Yellow Cover specification. This clock synthesizer provides a single chip solution for next generation Intel processors and Intel chipsets. ICS9LPR501 is driven with a 14.318MHz crystal. It also provides a tight ppm accuracy output for Serial ATA and PCI-Express support.
- **Detailed Spec check of the Clock buffer did not show any settings, that looked promising to help to solve the issue**

Crystal Problem ?

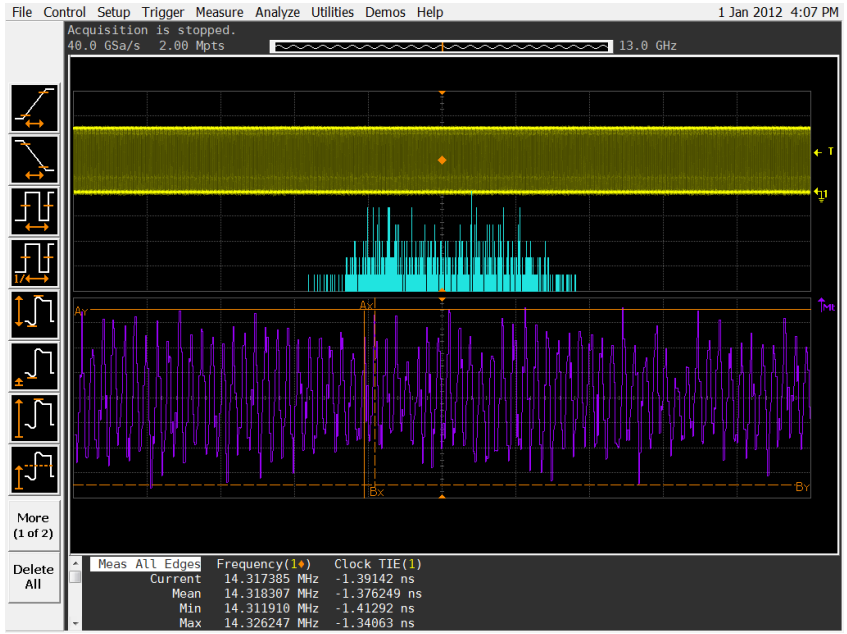
- **Removed Crystal Clock Oscillator at Controller to ensure this is not used …**
- **Frequency Tolerance of Crystal Clock oscillator at PLL:**
  - 14.318180 +-30ppm
    - Min Spec Frequency: 14.31775 MHz
    - Max Spec Frequency: 14.31861 MHz
- **Difficult to measure at crystal without distorting results due to Probe loading**
  - Crystal frequency was measured on Ref-Output of PLL
  - This could include PLL errors again (e. g. output drive due to Supply noise).
    - Output is specified with additional +- 100ppm

Crystal Problem ?

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

Measured:

- Min Frequency: 14.311 MHz (Spec: 14.317 MHz)
- Max Frequency: 14.326 MHz (Spec: 14.319 MHz)
- ~ 1.5MHz Modulation

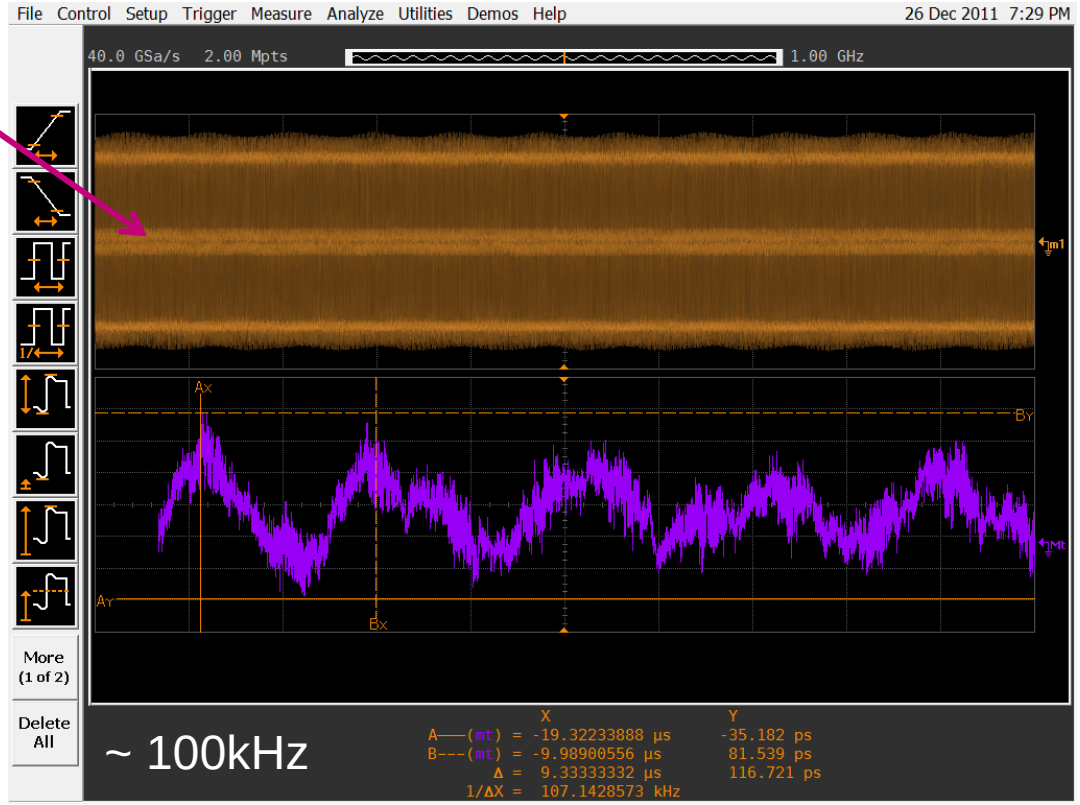


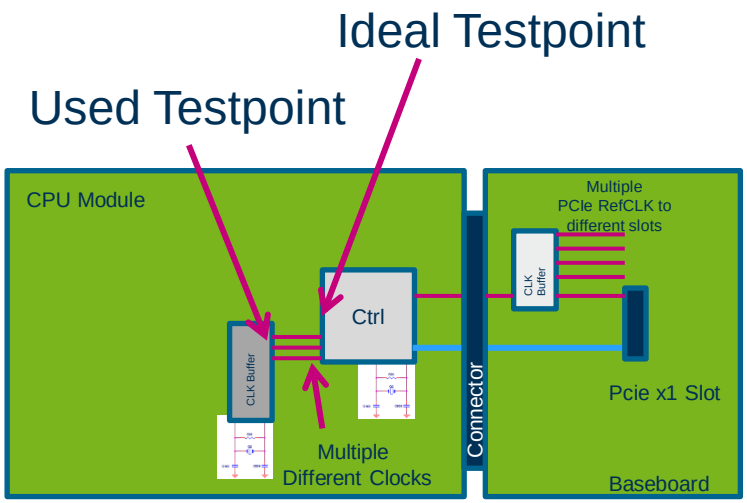
Might be something the can be analyzed in the future.
As no relation to 100KHz is seen we stopped at this point to check the crystal performance

PLL Clock out Problem ?

- **PLL CLK out was difficult to measure. Only Pins at the output are available as probe points!**
  - Change of Ref levels required
  - Reflections in Trace

Difficult Measurement, but 100KHz found again!





Agenda

1) Background and Motivation

2) Compliance Test Results

3) Eye diagram evaluation

4) SSC evaluation for TX and RefCLK

5) Follow back Data and Clock signal sources

6) Verify Power Supply noise

7) Test Results with Fix and Conclusion

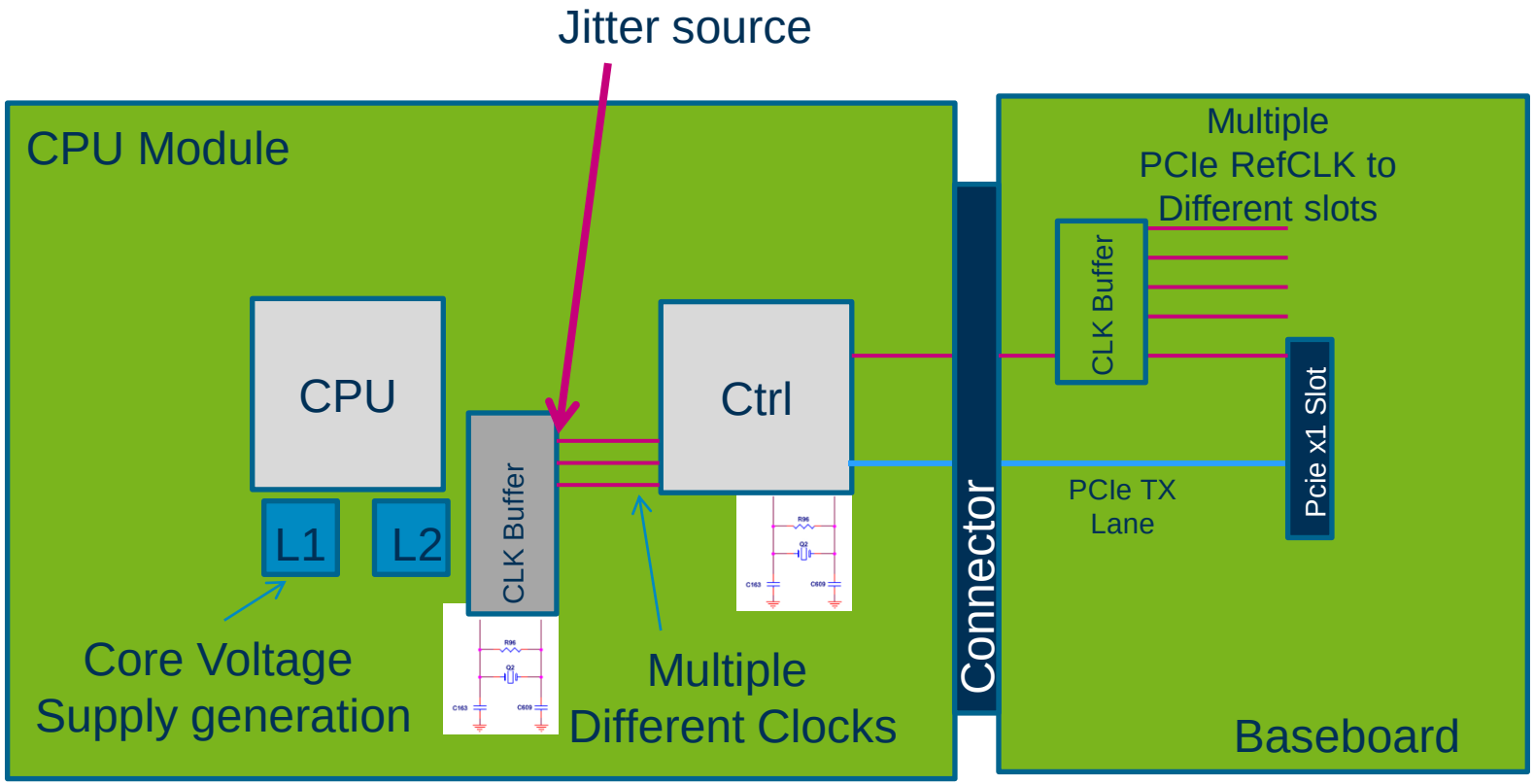
Status

- **TX Compliance test fail in UI width**
- **Jitter with ~ 100KHz Modulation seen on PCIe TX**
  - 100KHz is 3x Faster than SSC modulation with 33KHZ, therefore normal PLL will not follow this Jitter fast enough
- **Same modulation followed back the 100MHz Signature to Clock generator on CPU Module**
  - Crystal input for PLL seems not to be the problem
- **Next Suspects ?**

Noise from voltage Generators ?

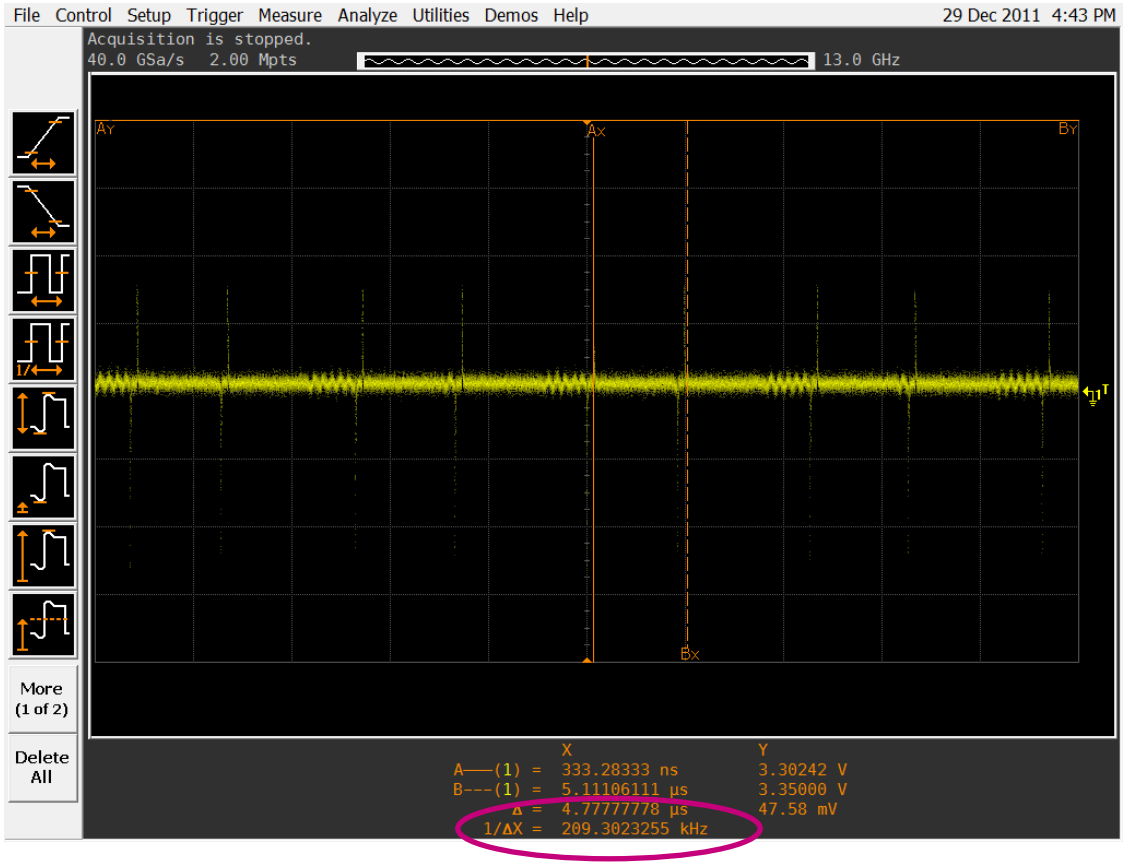
System Setup

- Core Voltage supply inductors are very close to the CLK Buffer



Emission above Voltage Regulators for CPU Supply

- **Shot in the Blue .. But 200KHz does not fit to our Problem ..**



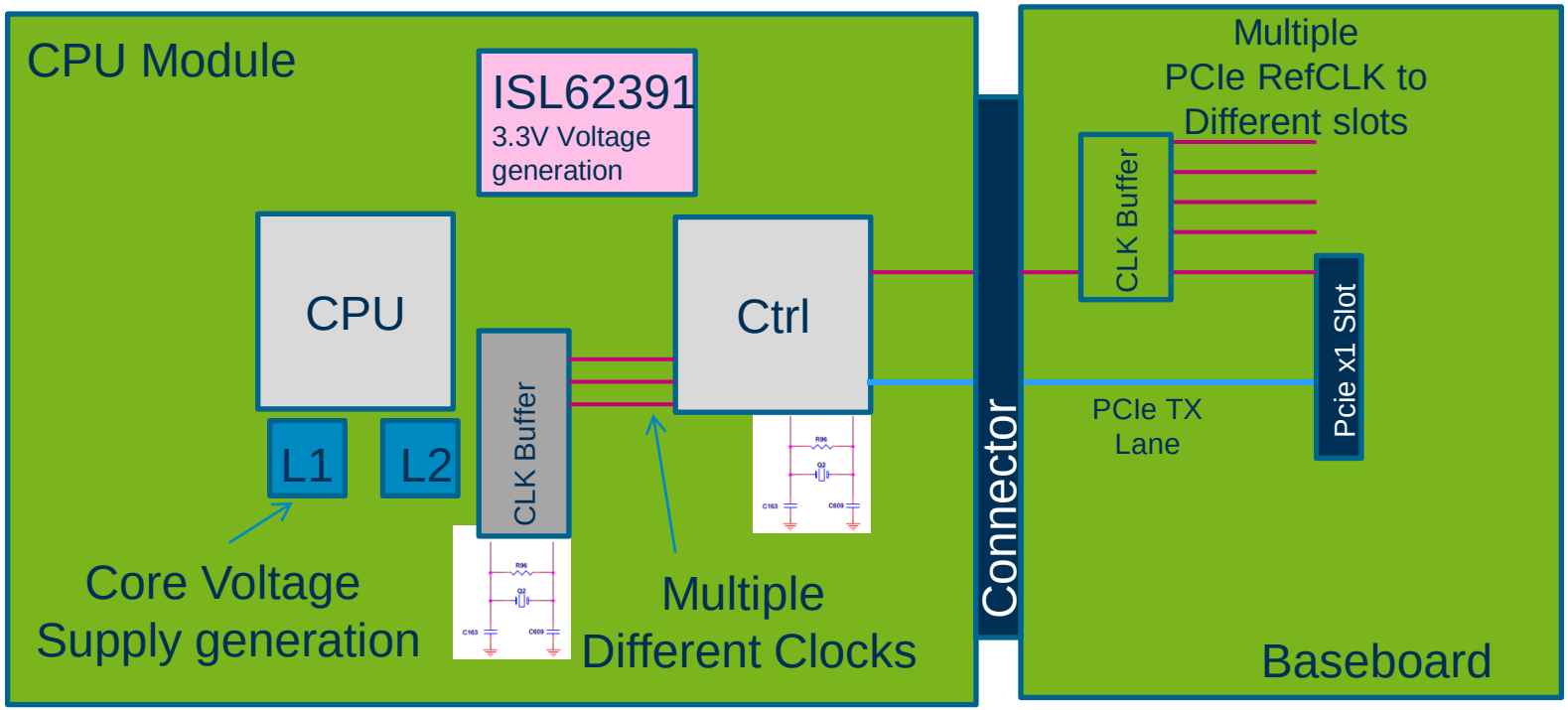
Just placed probe above Inductor …

Voltage supplies for PLL

- **Multiple supply rails of PLL**
  - 3.3V Filter1:
    - VDD_PCI (Pin 2)
    - VDD_48 (Pin 9)
    - VDD_Ref (Pin 61)
  - 3.3V Filter2:
    - VDD (Pin 16)
    - VDD_SRC (Pin 39)
    - VDD_CPU (Pin 55)
  - 1.1V:
    - VDD_IO
    - VDD_PLL3_IO
    - VDD_SRC_IO_1
    - VDD_SRD_IO_2
    - VDD_CPU_IO

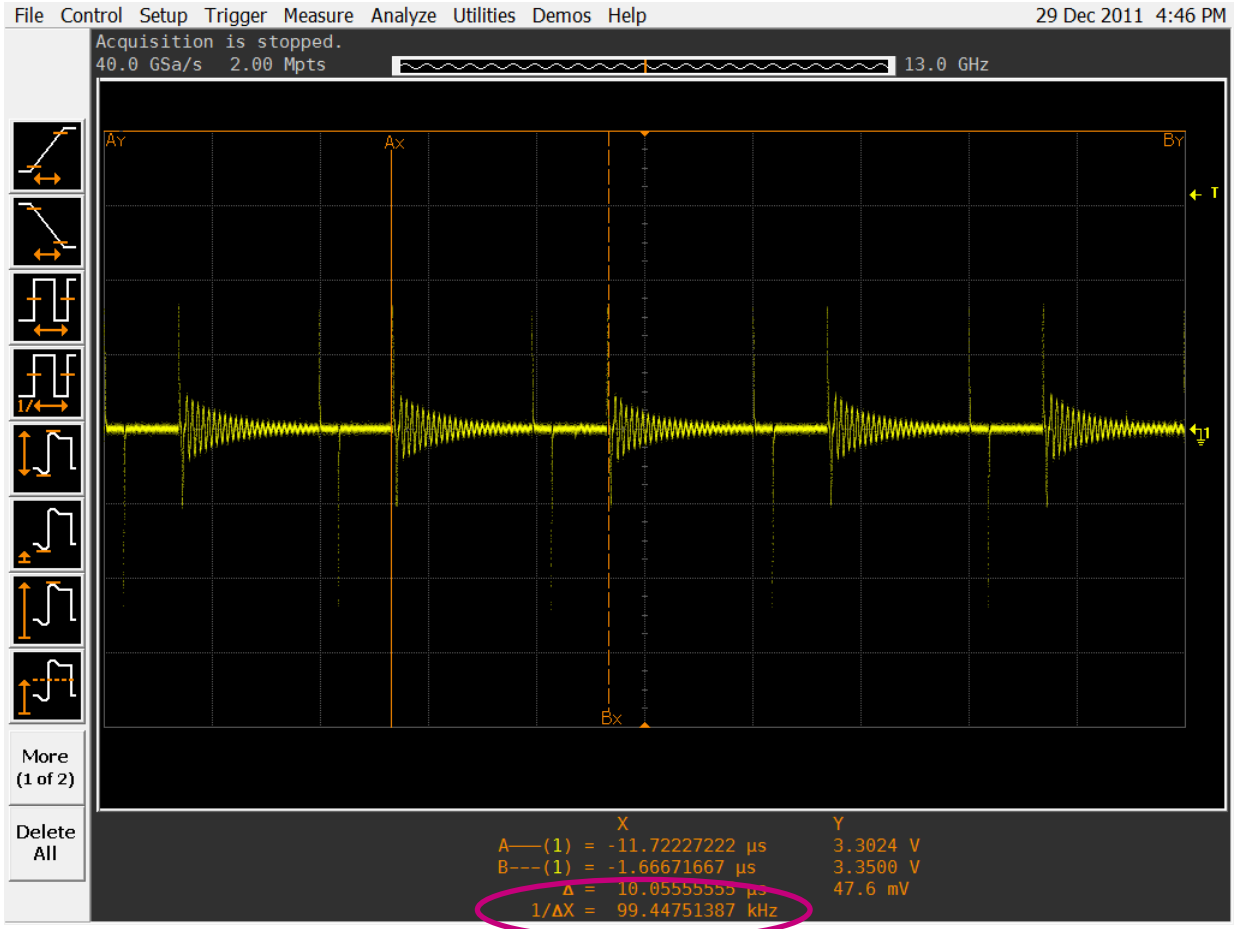
System Setup

PLL voltages are Supplied by ISL62391



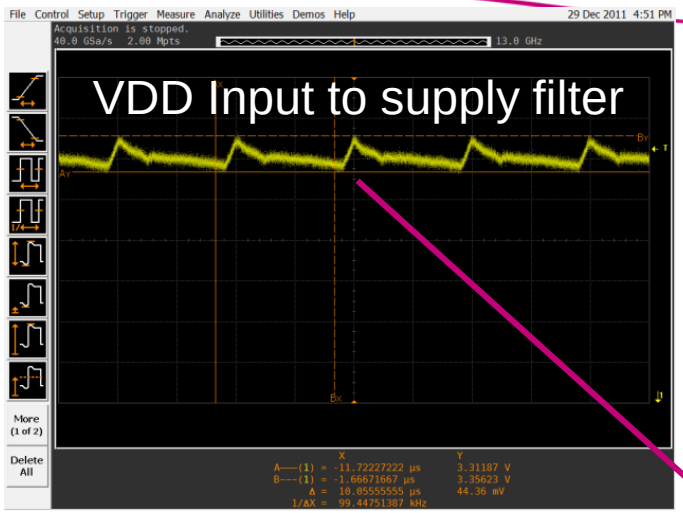
Emission above Voltage Regulators for PLL Supply

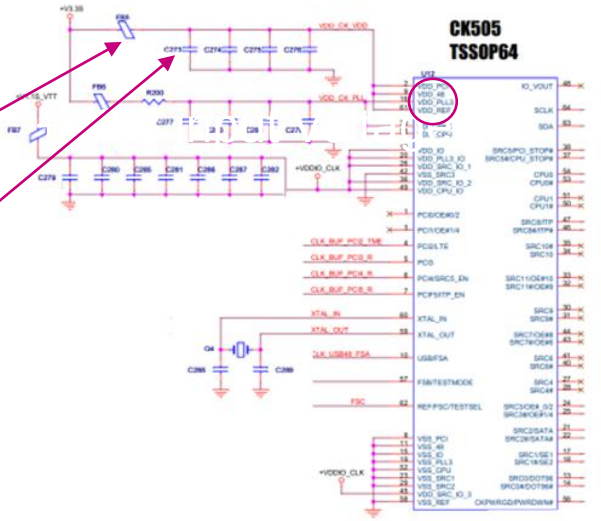
Emission above ISL62391 Voltage Regulator: 100KHz!



Regulator is far away ..
But seems related
to the Problem!

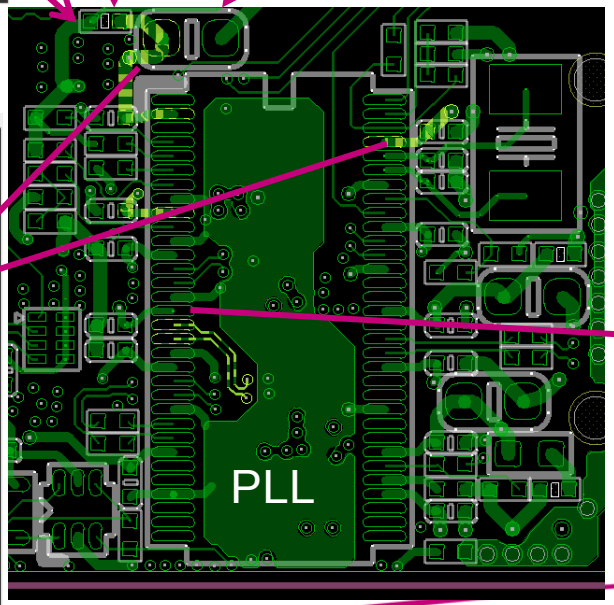
PLL Supply noise

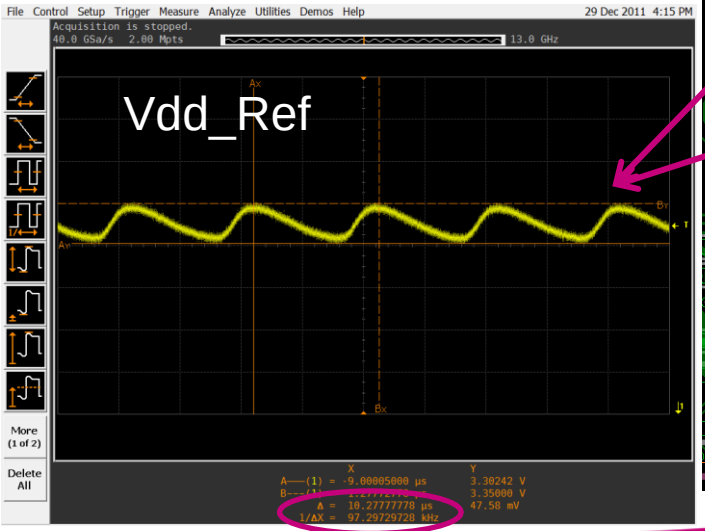


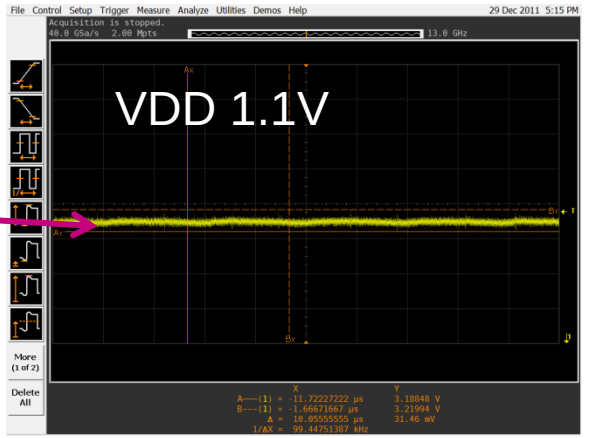


Ferrite Bead

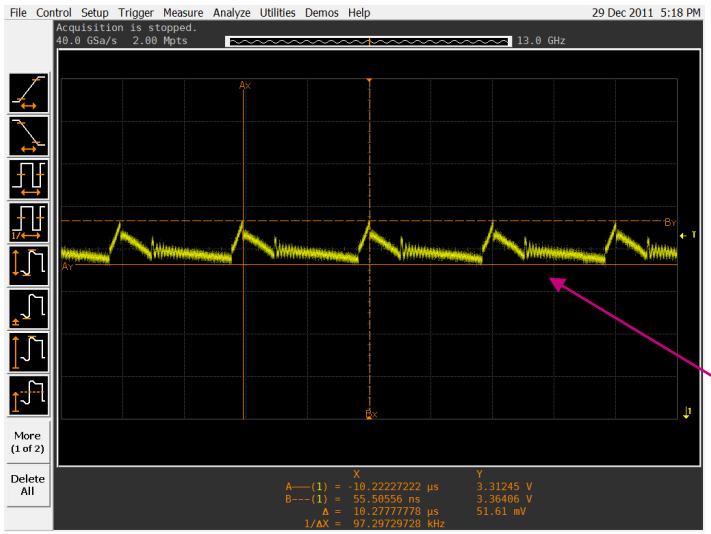
ByPass Cap

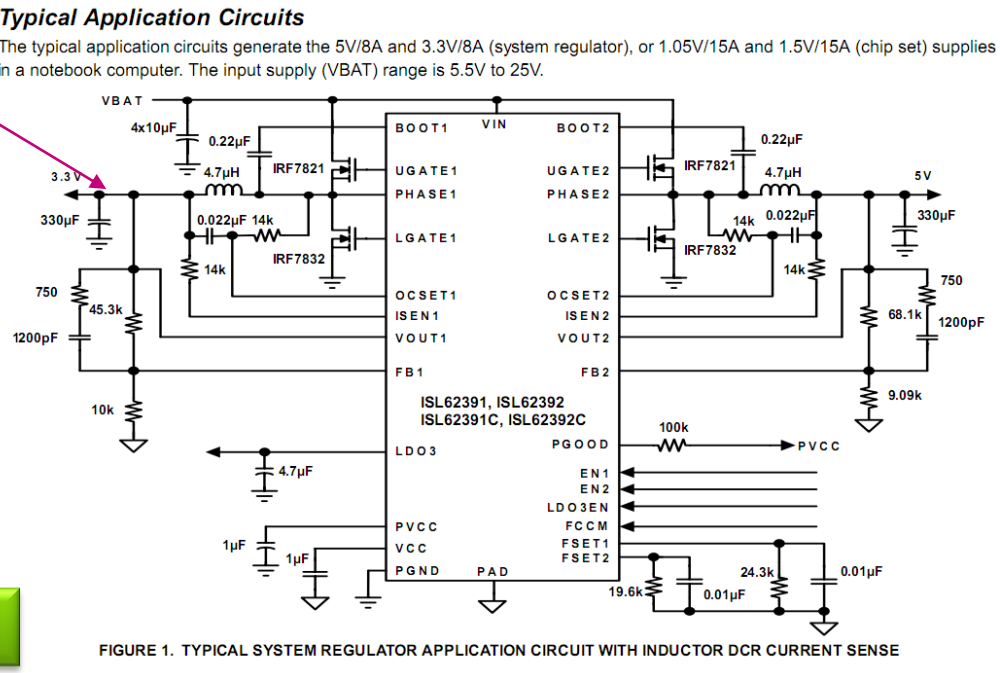






V33S @ C337 (source of V33S)



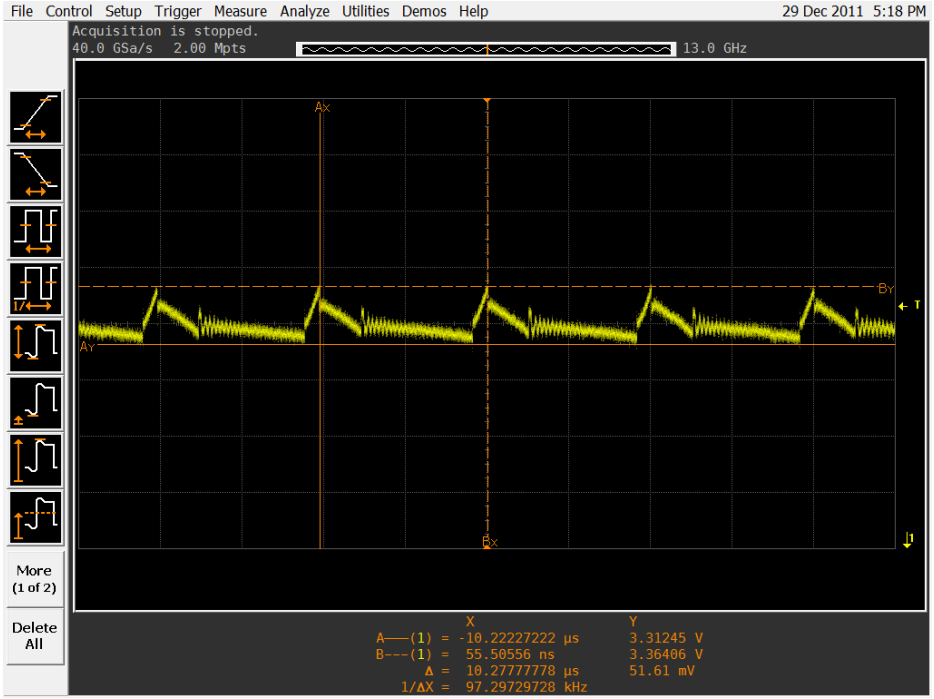


"Noise" is generated from ISL62391

Intersil ISL62391

DCM Mode Profiles

- Light-load efficiency is improved with period-stretching discontinuous conduction mode (DCM) operation.



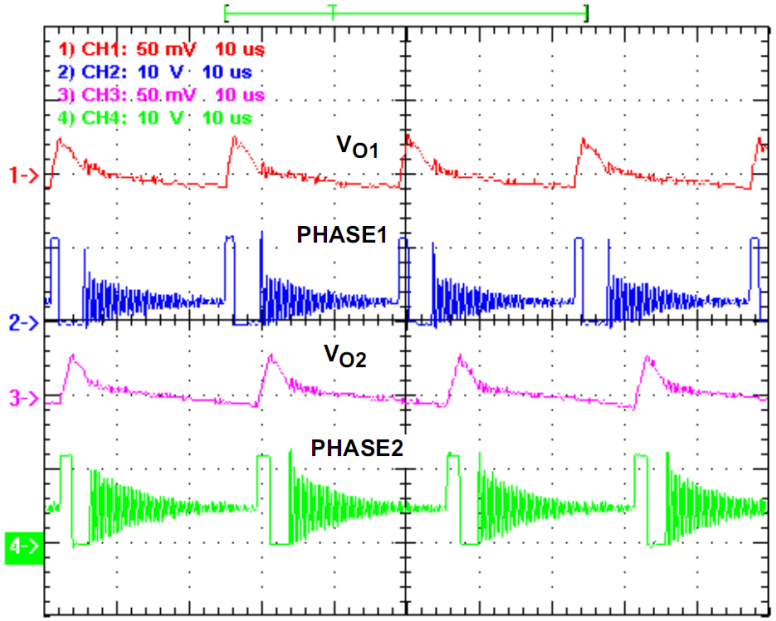


FIGURE 12. DCM STEADY-STATE OPERATION, V_{IN} = 12V, V_{O1} = 3.3V, I_{O1} = 0. 2A, V_{O2} = 5V, I_{O2} = 0.2A

Improvement Options

- **Now we know that the noise is generated from the Voltage regulator.**

- **Options for improvement:**
  - Adjust output Capacitor for Voltage Regulator
  - Optimize Ferrite Bead filtering of PLL input
  - Disable DCM mode

TIE improvement 1 by adding 2x 47uF at ISL62391 out

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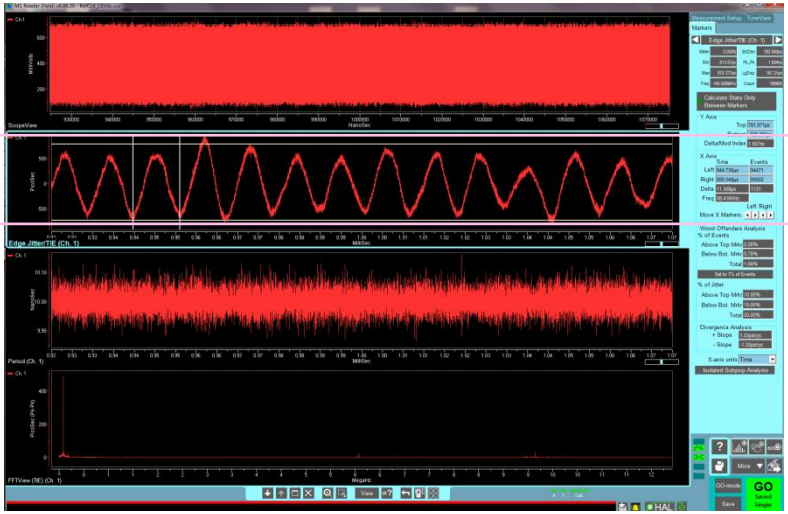
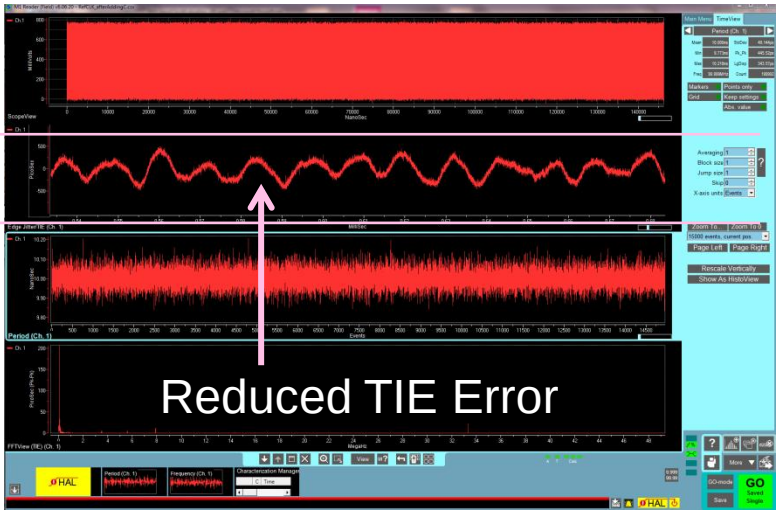
- Data Evaluation with ASA M1
- Original Vdd_Ck_Vdd
- New Vdd_Ck_Vdd with additional 2x47uF Cout on V33S

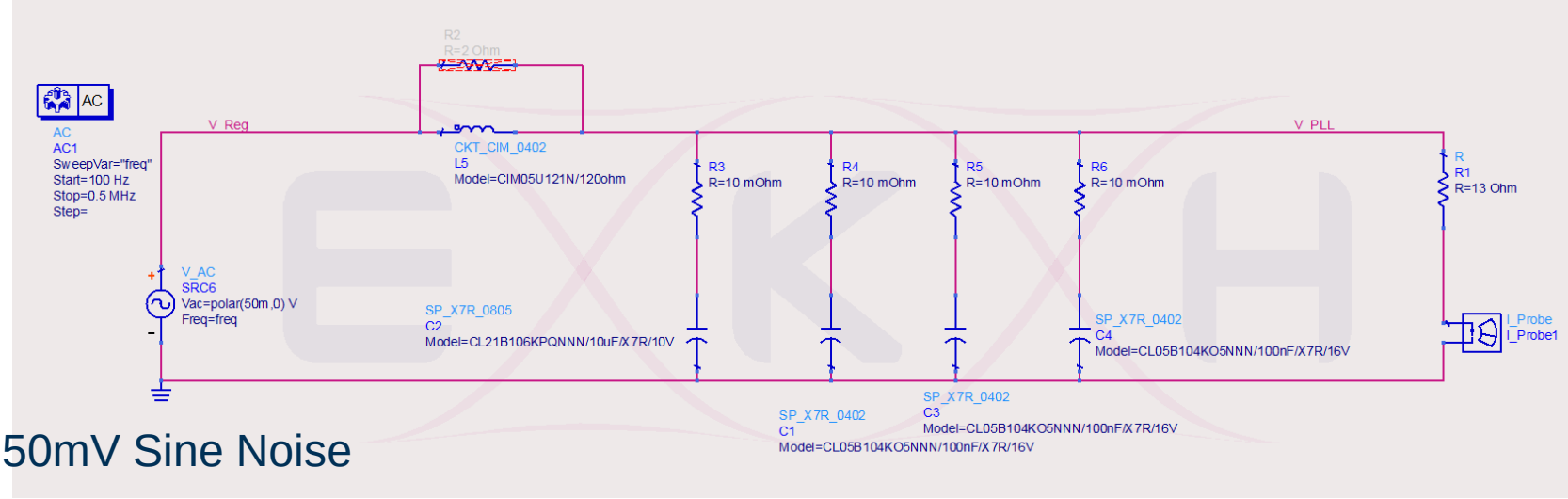




LC on the Regulator output can be optimized!

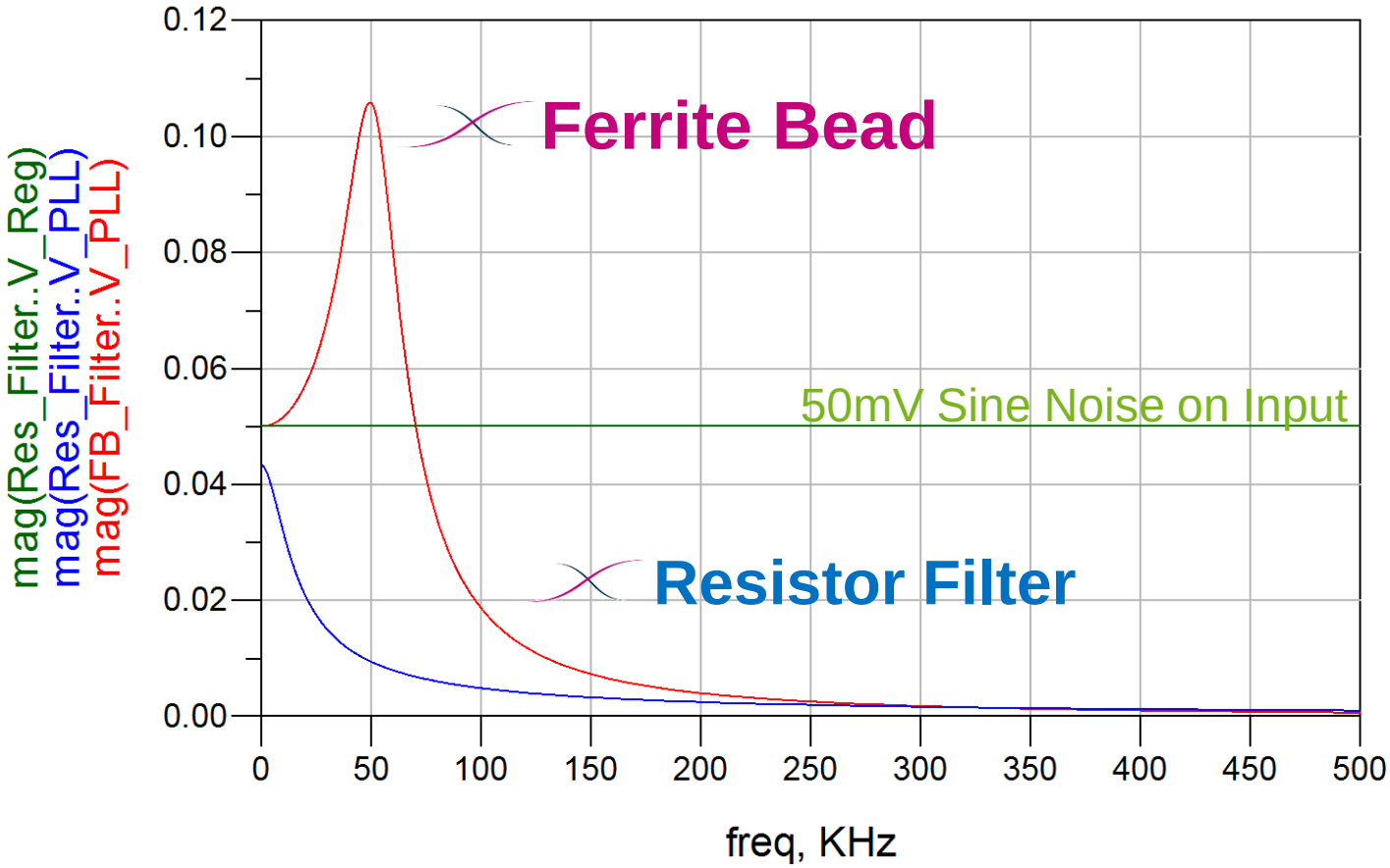
TIE improvement 2 by FB Filter optimization

- **AC Simulation with ADS**
  - Frequency Range from 100Hz to 500KHz
- **Components from Samsung ADS Library used**
  - Ferrit Bead and Capacitors on PLL Supply input
  - Resistors as ideal R modeled



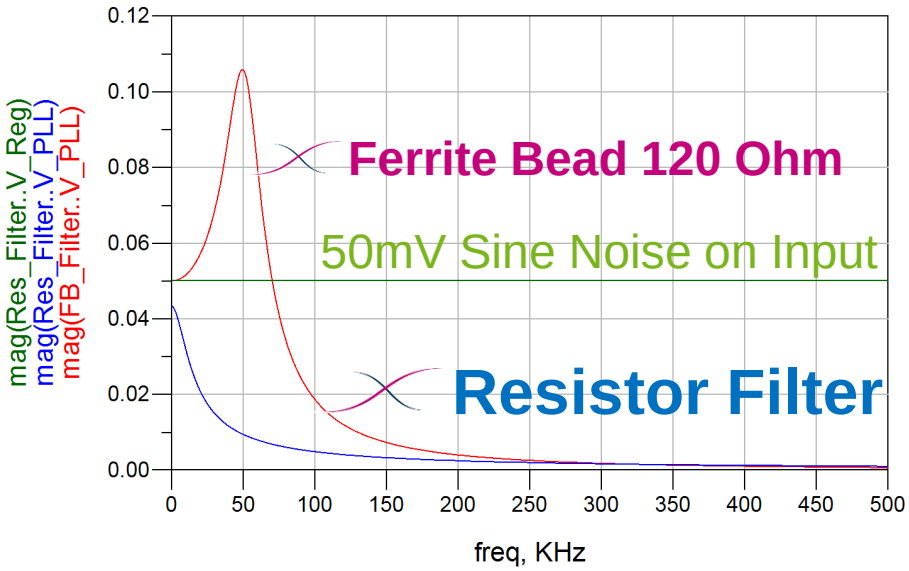
50mV Sine Noise

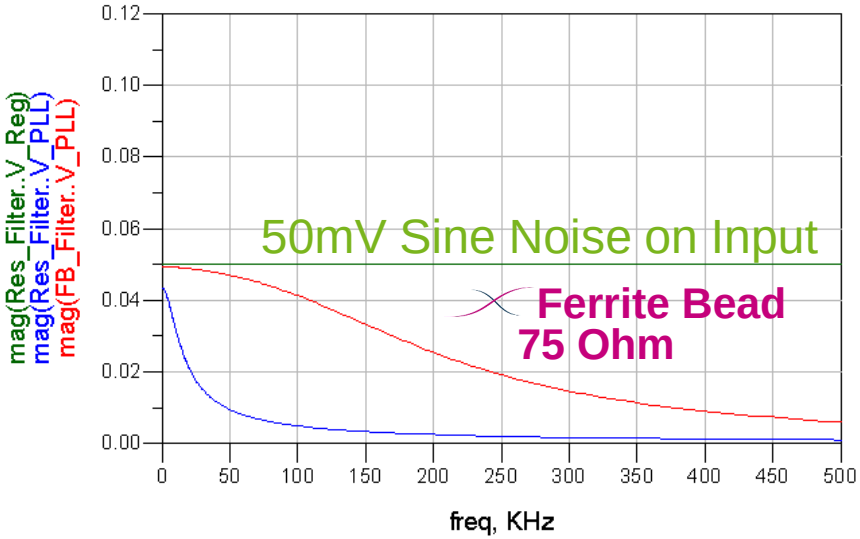
Power Filter Adjustment
Ferrite Bead vs. Resistive Filter



Power Filter Adjustment
Ferrite Bead change

- **Very often Ferrite Bead filter circuits are just copied from other designs without verifying that the circuit actually fits to the requirement!**





Resistor based filter
Caution required!

- **Required to check to ensure functionality and reliability!**
  - Voltage drop over Resistor based on drawn current
  - Resistor can handle burned power
  - Temperature of Resistor to ensure reliability

TIE improvement 3
Switch off DCM on VRM

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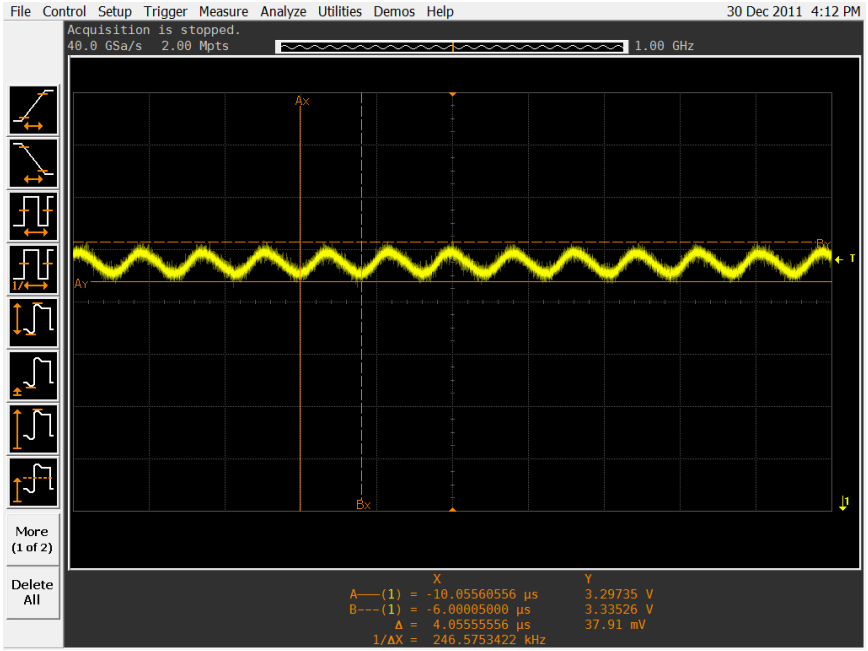
3.3V Supply before RC Filter



Intersil documentation

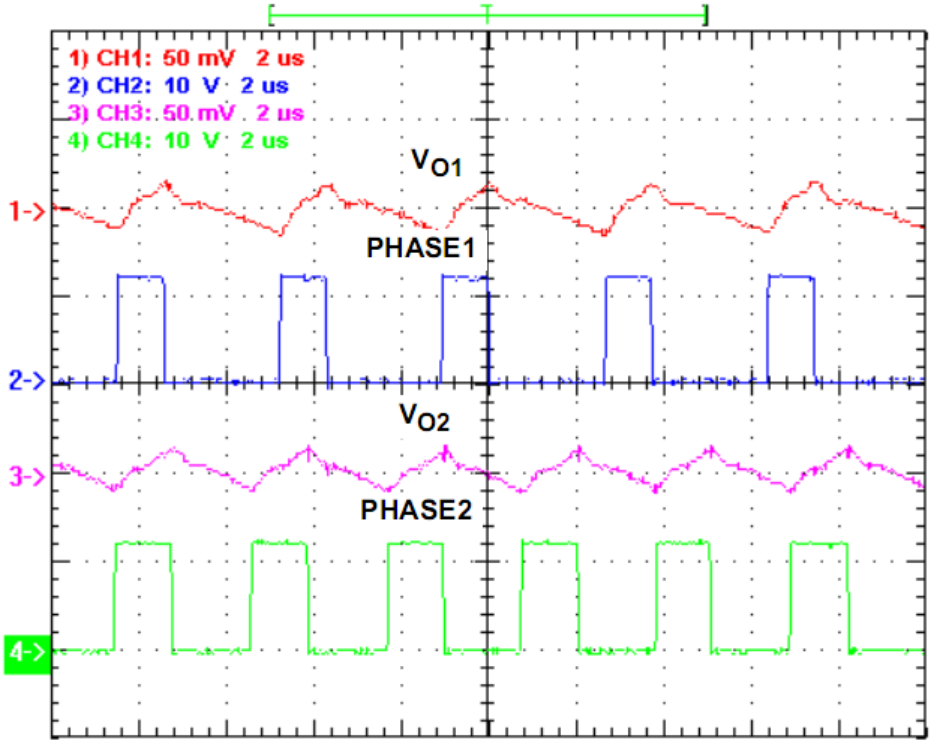
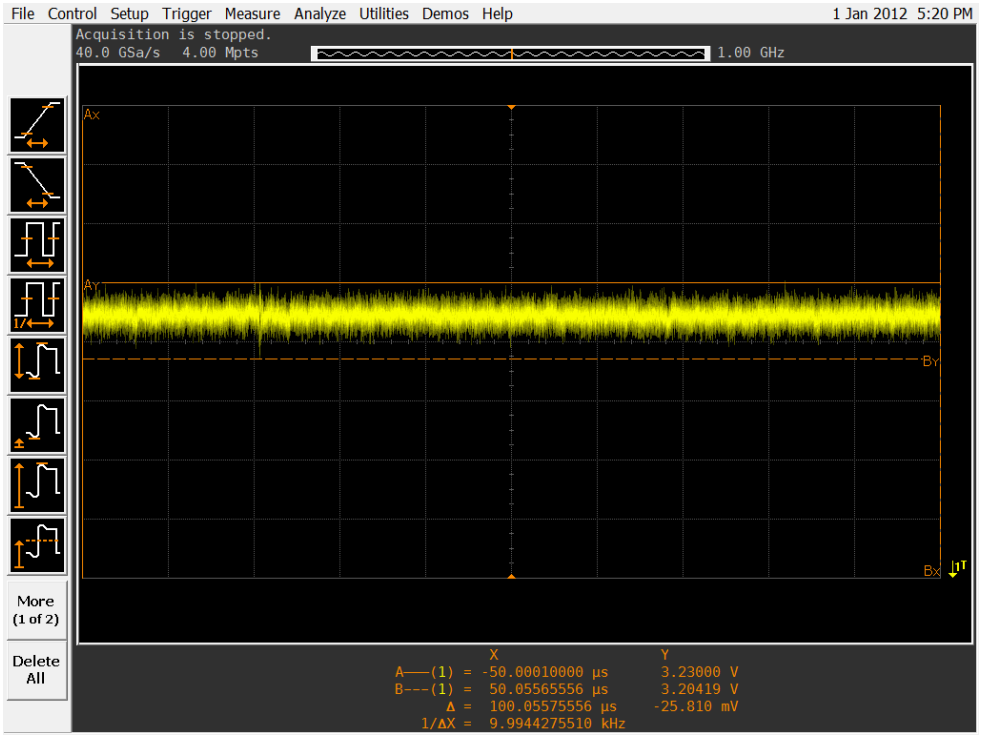


FIGURE 11. CCM STEADY-STATE OPERATION, V_{IN} = 12V, V_{O1} = 3.3V, I_{O1} = 5A, V_{O2} = 5V, I_{O2} = 5A

Supply Voltage after Resistor Filter

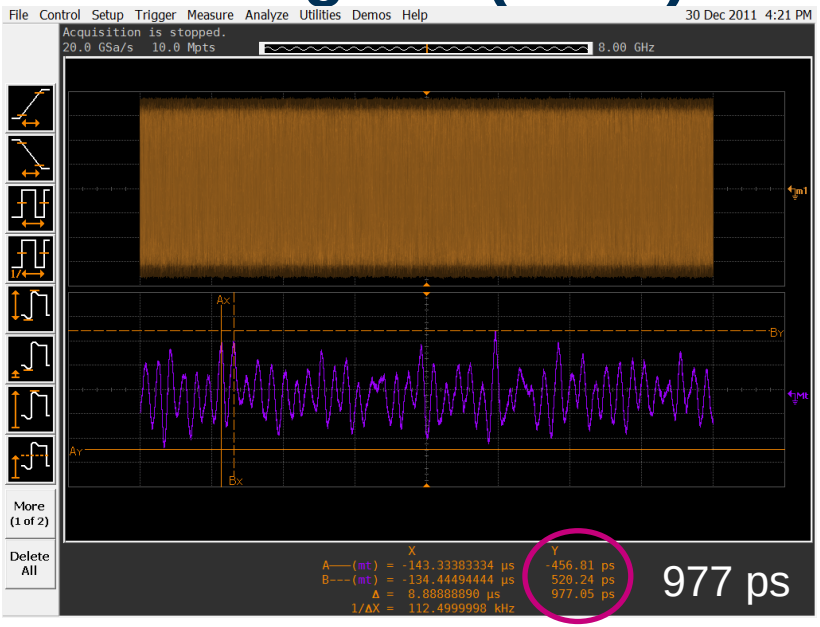
3.3V after RC Filter



250 kHz are filtered well!

TIE comparison

TIE original (DCM)



Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✗	1	1	System Board Tx, Unit Interval (PCIE 1.1)	399.8640ps	**-6.7 %**	399.8800ps <= VALUE <= 400.1200ps
✓	0	1	System Board Tx, Template Tests (PCIE 1.1)	0.000	50.0 %	Zero Mask Failures
✓	0	1	System Board Tx, Median to Max Jitter (PCIE 1.1)	69.96ps	9.1 %	VALUE <= 77.00ps
✓	0	1	System Board Tx, Eye-Width (PCIE 1.1)	263.94ps	7.3 %	VALUE >= 246.00ps
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)	485.2mV	22.8 %	274.0mV <= VALUE <= 1.2000V
✓	0	1	System Board Tx, Peak Differential Output Voltage (NonTransition)(PCIE 1.1)	480.0mV	24.0 %	253.0mV <= VALUE <= 1.2000V

TIE CCM mode (with FB)

Summary of Results

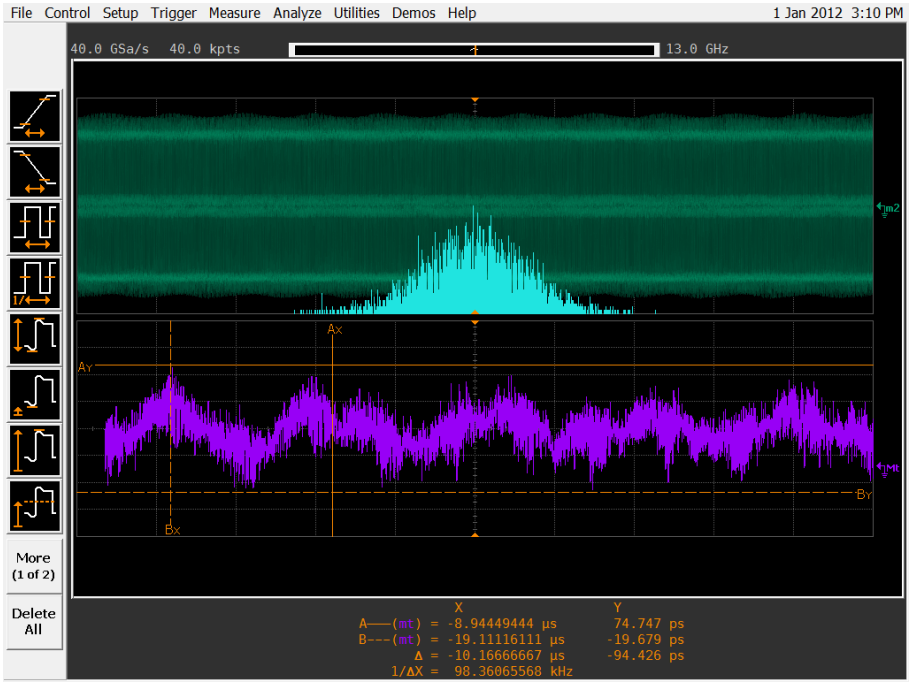
Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

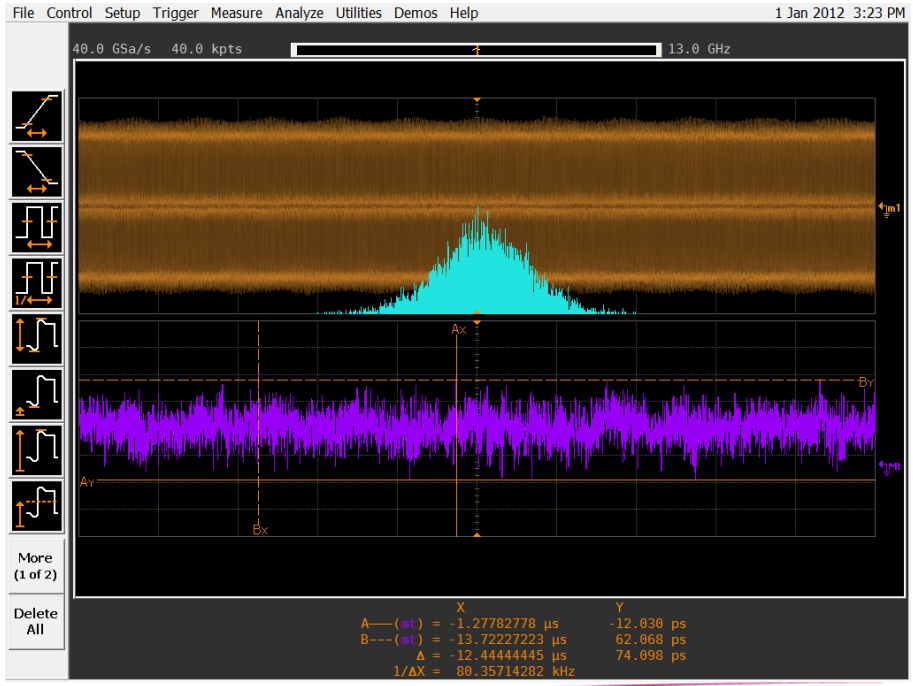
Still significant error, but 100kHz Modulation gone

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	System Board Tx, Unit Interval (PCIE 1.1)	399.8980ps	7.5 %	399.8800ps <= VALUE <= 400.1200ps
✓	0	1	System Board Tx, Template Tests (PCIE 1.1)	0.000	50.0 %	Zero Mask Failures
✓	0	1	System Board Tx, Median to Max Jitter (PCIE 1.1)	49.80ps	35.3 %	VALUE <= 77.00ps
✓	0	1	System Board Tx, Eye-Width (PCIE 1.1)	283.67ps	15.3 %	VALUE >= 246.00ps
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)	474.8mV	21.7 %	274.0mV <= VALUE <= 1.2000V
✓	0	1	System Board Tx, Peak Differential Output Voltage (NonTransition)(PCIE 1.1)	485.2mV	24.5 %	253.0mV <= VALUE <= 1.2000V

Source Clock for Controller

- **Clock Output from PLL**
  - Difficult to measure as measured at PLL, not at controller
- **Improvement in absolute TIE, but especially in 100KHz modulation!**





Agenda

1) Background and Motivation

2) Compliance Test Results

3) Eye diagram evaluation

4) SSC evaluation for TX and RefCLK

5) Follow back Data and Clock signal sources

6) Verify Power Supply noise

7) Test Results with Fix and Conclusion

Final Compliance test

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HIGH SPEED SIMULATION AND MEASUREMENT

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	System Board Tx, Unit Interval (PCIE 1.1)	400.0750ps	18.8 %	399.8800ps <= VALUE <= 400.1200ps
✓	0	1	System Board Tx, Template Tests (PCIE 1.1)	0.000	50.0 %	Zero Mask Failures
✓	0	1	System Board Tx, Median to Max Jitter (PCIE 1.1)	48.97ps	36.4 %	VALUE <= 77.00ps
✓	0	1	System Board Tx, Eye-Width (PCIE 1.1)	294.87ps	19.9 %	VALUE >= 246.00ps
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)	505.8mV	25.0 %	274.0mV <= VALUE <= 1.2000V
✓	0	1	System Board Tx, Peak Differential Output Voltage (NonTransition)(PCIE 1.1)	511.0mV	27.2 %	253.0mV <= VALUE <= 1.2000V

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✗	1	1	System Board Tx, Unit Interval (PCIE 1.1)	400.1650ps	-18.8 %	399.8800ps <= VALUE <= 400.1200ps
✓	0	1	System Board Tx, Template Tests (PCIE 1.1)	0.000	50.0 %	Zero Mask Failures
✓	0	1	System Board Tx, Median to Max Jitter (PCIE 1.1)	66.75ps	13.3 %	VALUE <= 77.00ps
✓	0	1	System Board Tx, Eye-Width (PCIE 1.1)	266.28ps	8.2 %	VALUE >= 246.00ps
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)	464.5mV	20.6 %	274.0mV <= VALUE <= 1.2000V
✓	0	1	System Board Tx, Peak Differential Output Voltage (NonTransition)(PCIE 1.1)	495.5mV	25.6 %	253.0mV <= VALUE <= 1.2000V

Final Compliance Results
TX at PCIe Slot

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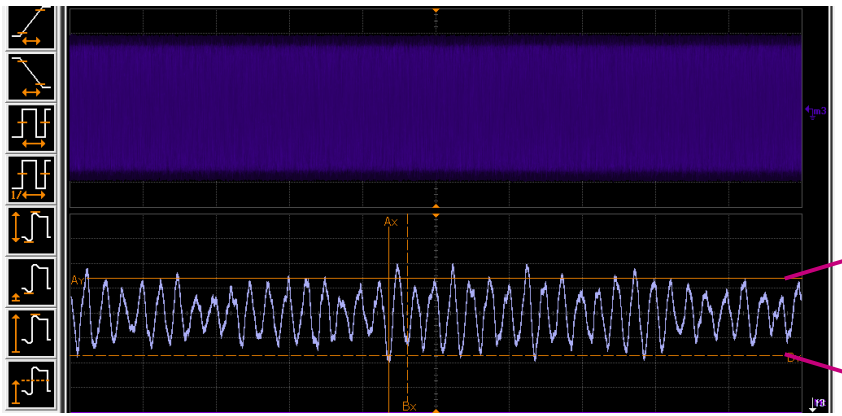
HIGH SPEED SIMULATION AND MEASUREMENT

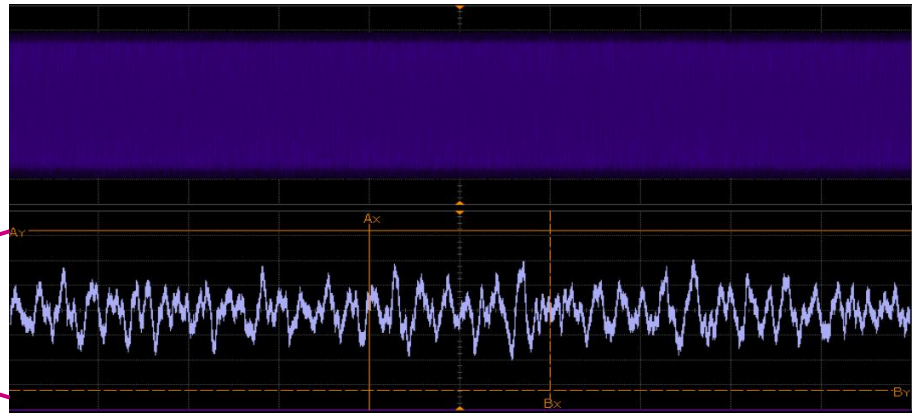
UI Time Trend comparison with all changes

- Quite some margin in the TX UI Time Trend
- There might be some more Improvement possible, but TX compliance test passes.

Original Result



Improved Result



Conclusion

- **Root Cause is “Power Noise” that was converted to jitter**
  - This Jitter was just too fast to allow the PCIe1 PLL to follow it.
- **Due to Power delivery improvement the PCIe compliance Test result could be improved a lot**
  - Change of PLL Power Filter to RC filter was helping most
  - Switch to CCM mode of Voltage generator was done, but not really required.
- **Even with this fix there might be some additional option to improve the Jitter behavior**
  - The TIE from this setup looks different to other reference TIE Measurements and still somehow modulated

The Jitter was the murder of our Signal, but the real bad guy who suborned the Jitter was the power Supply!

Required KnowHow

- **Detailed Knowledge of**
  - PCIe Specification
  - Probing (high speed and Crystal)
  - Scope handling
  - Scope compliance Measurements
  - PLL behavior and specification
  - Crystal behavior and specification
  - Supply filtering
  - Supply generation

Backup

Company Facts

- **Founder:**
  - Dipl. Ing. (FH) Hermann Ruckerbauer
- **Founded:**
  - March 2009
- **Location:**
  - Office in Moos (Bavaria), Germany
- **Network partners in:**
  - Munich (Design, Layout, CAD)
  - Straubing (EMV)
  - Deggendorf (Lab)
  - China (Shandong und Shaanxi): Oulong Consulting

Hermann Ruckerbauer
Background

- **Study of Micro System Technology at University of Applied Sciences in Regensburg**
  - Dipl. Ing. (FH) Micro System Technology
- **15 Years experience in Memory Development and High Speed Signaling**
  - Siemens: Bench and Production test
  - Infineon / Qimonda:
    - High Speed Signaling
    - Application test
    - Interface standard definition
- **Holder of many patents**
- **IEEE Publication:**
  - Cascading Techniques for a High-Speed Memory Interface

EKH Services

- Consulting for High Speed Signaling
- Consulting for memory implementation
- High speed simulation and measurement
- Power delivery simulation
- Model generation
- Logic Analyzer measurements
- Failure analysis (esp. on memory interfaces)
- PCB Design and Layout