EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

Knowing the Limits!

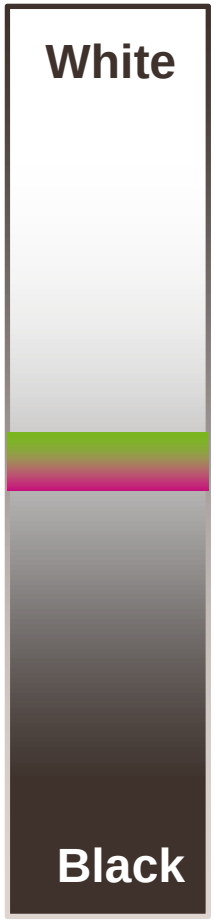
Design Optimization and Tradeoff between Performance and Cost

Knowing the Limits

Black or White in high speed “digital” ?

- **“Digital” means the Transmitter tries to send “0” and “1” bits only and the Receiver recognize “0” and “1” information only, but the Signal between Transmitter and Receiver is analog!**

There is no Black or White for high speed digital signals!
Just different levels of grey!

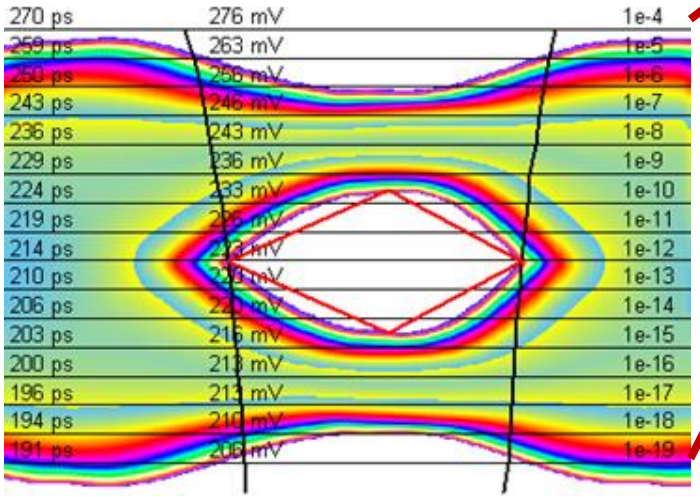


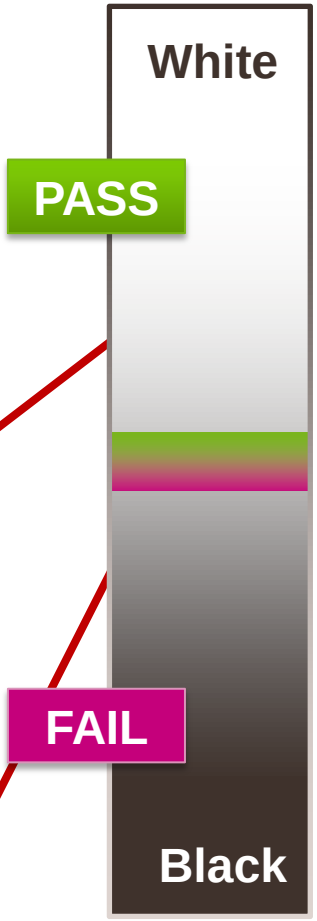
- **It is important to know where a design is located on this grey scale!**
- **In some point it does not help to shift the Design from white to even “more white”, but it is important to know how far the design is away from the Pass or Fail boarders.**

Knowing the Limits
Pass or Fail ?

- **Each signal and each device has it's own position and pass fail boarder on this scale**
- **With increasing speeds the margins are getting smaller and smaller.**
  - It is getting more and more important to know where the limit is!

For High Speed signals even the Pass/Fail region is characterized by the BitErrorRate





Knowing the Limits

Where is your design on this scale?

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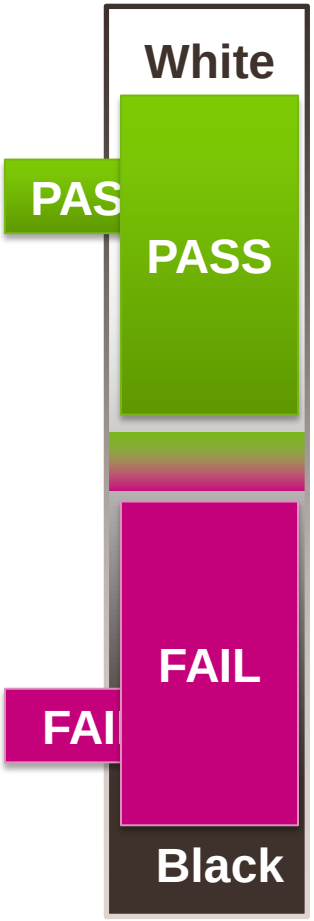
- **Compliance test just result in “Pass” or “Fail”, but don’t give any additional information:**
  - Being in the White area is good …
    - But the Compliance test gives no information how far the design is away from the Pass/Fail boarder?



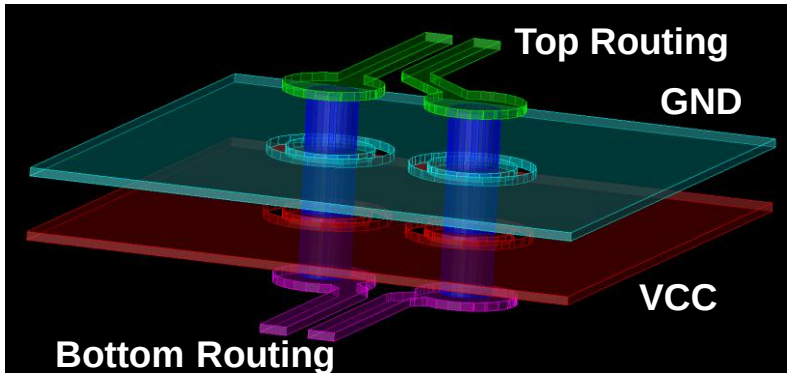
Being far away from the Pass/Fail region in the “White” area means to deliver performance that is not needed and will not be paid by the customer.

The product can be optimized for cost!

  - Being in the Black area means that problem solving in firefighting mode is needed!
    - The compliance test has no information on the fail reason!

Knowing the Limits
Optimization based on Experience

- **Controlled impedance routing is possible with GND or VCC referencing, but switching the reference can be critical!**
  - Most stackups today serve single ended and differential signals, so even for differential signals a significant part of the return current (and the impedance) are relying on the reference plane!
- **Possible Issues:**
  - +20% impedance change on top and -20% impedance change on bottom can happen even for impedance controlled designs!
    - Limit number of vias to limit the possible impedance steps
  - Missing current return path between Top and Bottom routing
    - Place AC coupling capacitor between GND and VCC close to the Vias.



Knowing the Limits
Optimization based on Experience

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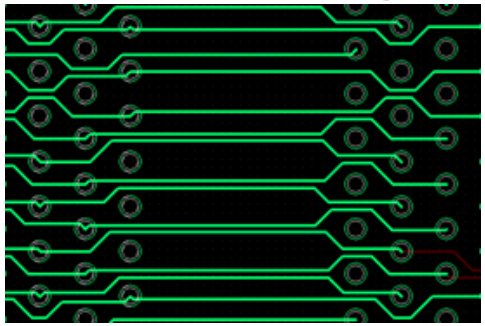
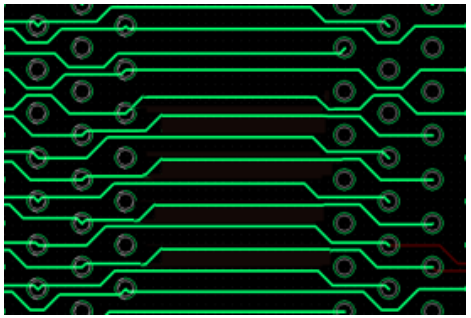
- **Just doing a quick job can result in the trace routing shown in the right picture**
  - Long routing with critical spacing



- **Spending some minutes more on routing can reduce the X-talk by better distributing the traces like in the lower picture**
- **But is this resource invest really required or just shifting the design from “White” to “even Whiter” area on the Greyscale ?**



Design by experience can shift the design on the greyscale, but the absolute location on this scale is unknown!

Knowing the Limits
Simulate to Quantify!

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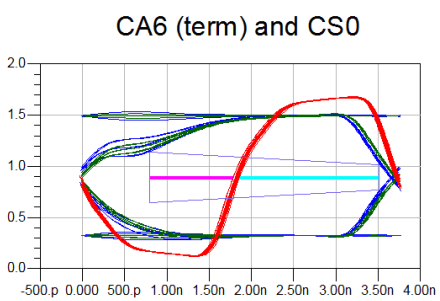
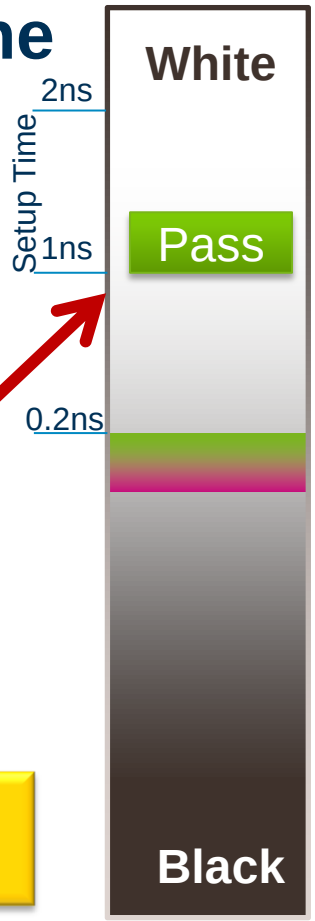
- **Doing some transient simulation allows to get a first knowledge and quantify the quality of the design and the location on the greyscale!**
  - Simulation can give MHz, ps or mV numbers!
  - This numbers can be compared with the device requirements or even used in a Timing Budget.



Default_Dataset_Name	
CLK_CA_100um_1x5_2Vns	

indep(caltst1)	caltst1
Setup time[0]	991.1 p
Hold time [1]	1.650 n
Diff Clock skew [2]	80.36 p
Valid window [3]	2.721 n
CLK skew start[4]	1.783 n
CLK skew end[5]	1.864 n
Valid window end[6]	3.514 n
Valid window start[7]	792.1 p
Delay[8]	1.619 n
vref[9]	890.0 m



Even during the design phase we do have a feeling how far the final design will be away from the Pass/Fail border.

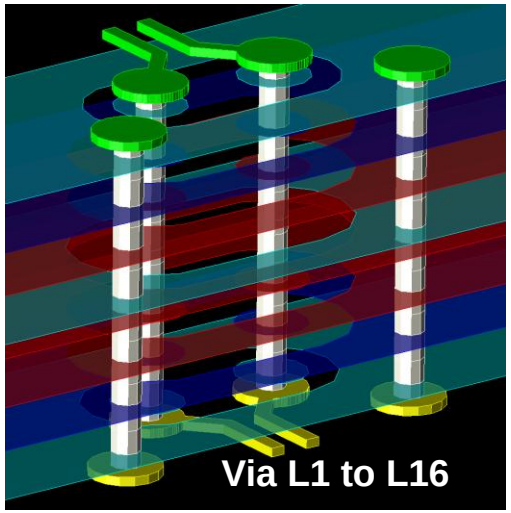
Knowing the Limits
Optimize the design for cost!

- **If the distance to the Pass/Fail is big enough we can now for the first time optimize the Design for Cost!**
- **Having enough margin can be used to**
  - Reduce trace spacing
  - Select simpler technology (e. g. no blind vias)
  - Remove Termination regulators (e. g. for a DDR2 CA bus)

Although there is still no Black and White the knowledge out of simulation can be used to do cost optimization and/or performance improvement!

Knowing the Limits
Optimize the design!

- **We still do not know the exact location, as any simulation is just as accurate as the models used**
- **More accurate models can be generated by using a 3D field solver, e. g. for via modeling**
- **This models can be used for:**
  - Accurate models for time domain simulations
  - Check the requirements for advanced technology like backdrilling or blind/burried vias.



Knowing the Limits!
Parasitic optimization

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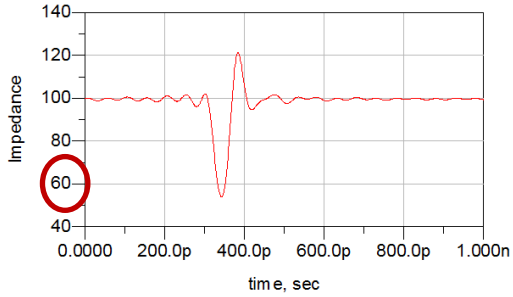

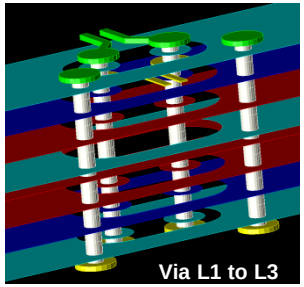

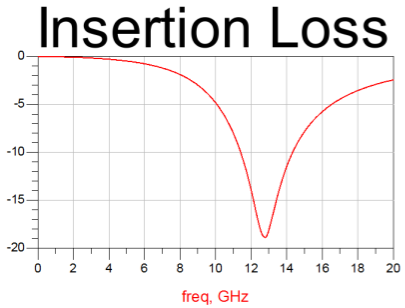

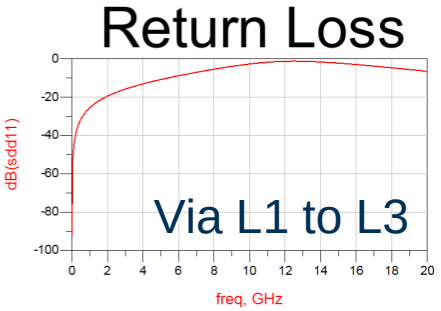

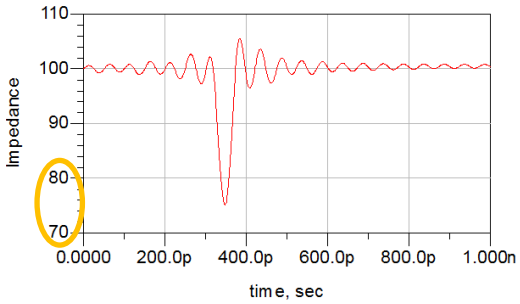

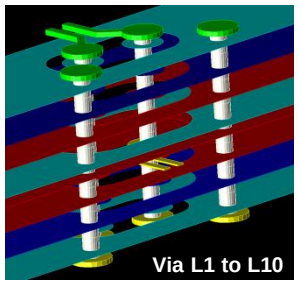

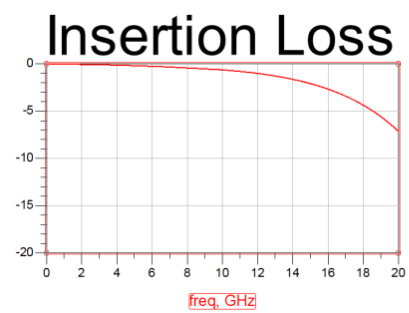

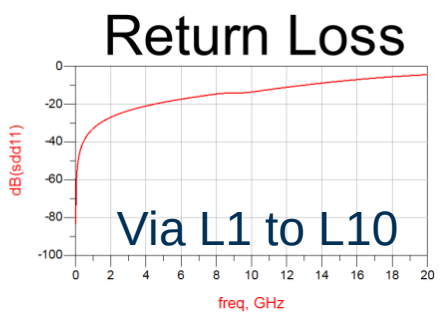

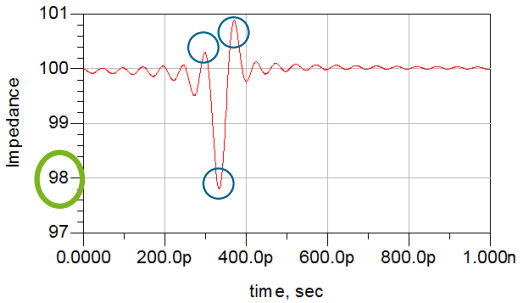

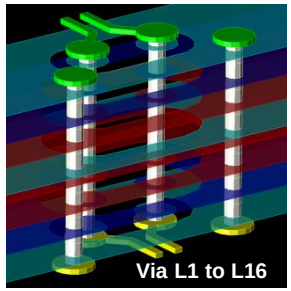

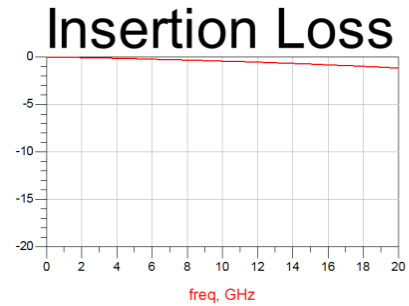

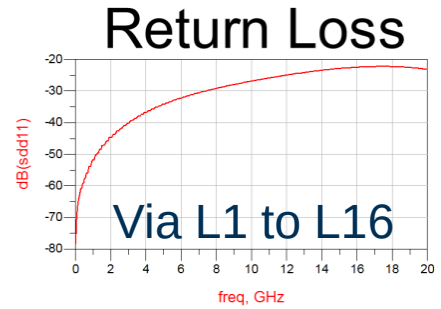

Knowing the Limits!

Stackup based on real SI needs!

- **Signal Integrity might allow to reduce the cost by reducing the layer count in the stackup.**
- **The following two stackups do have the same amount of Signal and Power Layers but still some differences**
  - “Perfect” Stripline vs. Asymmetric dual Stripline
  - Power referencing of two signal layers
  - Reduced number of GND layers

Is it possible to implement Power Delivery with the cost optimized stackup ?

“Perfect” Stackup

L1 Top	Microstrip	Sig
L2		GND
L3	Stripline	Sig
L4		GND
L5	Stripline	Sig
L6		GND
L7		Power
L8		Power
L9		GND
L10	Stripline	Sig
L11		GND
L12	Stripline	Sig
L13		GND
L14 Bottom	Microstrip	Sig

L1 Top	Microstrip	Sig
L2		GND
L3	Asymmetric dual Stripline	Sig
L4	Asymmetric dual Stripline	Sig
L5		Power
L6		Power
L7	Asymmetric dual Stripline	Sig
L8	Asymmetric dual Stripline	Sig
L9		GND
L10 Bottom	Microstrip	Sig

Cost optimized Stackup

Knowing the Limits!

From Signal to (DC) Power Integrity!

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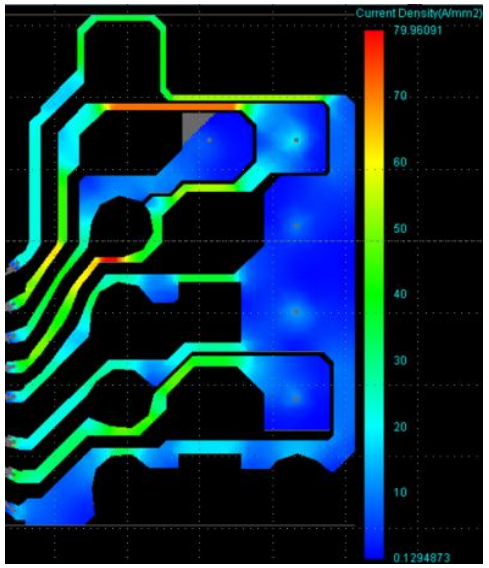
- **Trying to reduce the layer count requires to think about Power Delivery implementation**
- **For simple structures a DC-IR drop calculation can be done**
- **For more complex structures the Layout Tool has features to calculate:**
  - Max. Voltage drop
  - Max. Current density

DC IR-Drop Analysis verifies Power routing with reduced number of layers!



DC-IR Drop Calculation Current Density Plot

Knowing the Limits!
AC Power Integrity!

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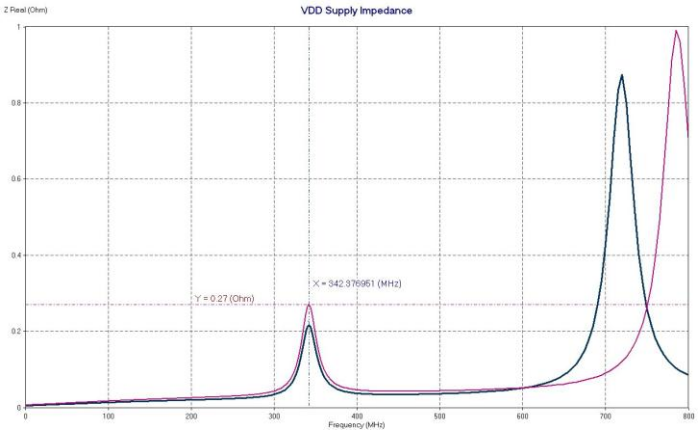
- **AC Power integrity should be verified as well and can be used to reduce cost.**
- **This is done by a plot "AC impedance over Frequency"**
- **This analyses checks and allows to optimize:**
  - Number of decoupling capacitors
  - Value of decoupling capacitors
  - Quality of decoupling capacitors
  - Shape of Power/GND planes



Knowing the Limits
Conclusion

- **Tools for finding the Limits of a Design**
  - Experience, Experience, Experience!
  - Transient (time domain) Signal Simulation
  - Frequency Domain Simulation for
    - Optimization of critical structures
    - Model generation of critical structures
  - DC Power Delivery
    - Voltage Drop
    - Current density
  - AC Power Delivery:
    - Impedance over Frequency

Knowing the Limits
Conclusion

- **Possible areas for improvement when knowing the Design Limits:**
  - Routing area reduction
  - Stackup Layer count reduction
  - Use cheaper manufacturing technology
  - Passive component reduction
    - Termination resistors
    - Decoupling capacitors
  - Active component reduction
    - Termination Regulators

Knowing the Limits
Conclusion

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HIGH SPEED SIMULATION AND MEASUREMENT

“Knowing the Limits” of a design allows to generate reliable products AND to reduce cost without compromising performance!

It is essential to plan for this already during project setup phase!

This is not a topic for a single project, but needs to be part of a companies strategic planning!