

ADS User Group Meeting Sept. 28th 2010 Andover (MA)



1) Introduction

2) Analog/RF Schematic Simulations

3) 3D Multilayer EM for Momentum

4) Data evaluation with the Data Display

5) Arbitrary 3DEM for FEM and FDTD Elements in EMPro and ADS

6) FrontPanel routines

7) Conclusion

8) Backup

1) Introduction ADS: The Swiss army knife of EDA



- imes "Signal Integrity" (SI) covers a wide range of topics!
- X There are a lot of different tools out that cover parts of the topics included in SI. Using different tools means:
 - Learn new handling for each tool!
 - A lot of Import/Export tasks are required!
- \times EKH uses ADS as single solution for all signal integrity related investigations.

Memory interfaces (e. g. DDR2 / DDR3 …)

- High speed interfaces (e. g. PCIe, 10Gb Ethernet...)
- X This presentation gives an overview how we use ADS combined with some of our Tips and Tricks!



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2) Schematic Simulation

The Multilayer Transmission line Library

Schematic based simulation can often replace layout based simulations

- X EKH does many simulations based on the Multilayer transmission line library.
 - Even "Post-Layout" simulations are done by rebuilding the topology with this models
 - Good engineering judgment is required to implement an accurate representation of the layout
 - Selecting "representative / mean" values for Spacing / Length
 - Does the Transmission line model cover the behavior of the real Layout (e. g. slots in reference planes)?

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2) Schematic Simulation The Multilayer Transmission line Library



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2) Schematic Simulation Stackup definition



 \times Stackup definition is not that simple, so we generated some templates to simplify the process.



Once the Stackup is defined all variables will be
 hidden
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2) Schematic Simulation **Stackup definition**



Physical view of the Stackup

> Physical view is drawn in ADS on additional layers

				Stackup 6	laver incl. co	onfor
L1 blank	t1 = + 0um					
L2 Signal	t2 = + 43um	er1 = 3.8	H1 = t2 + 1um	Vetal-1 Dielectric-1		Var Egn
100 u	m	er2 = 4.1	H2 = 100um	Meail-2 Meail: TJ. concj. Trifiji		-
L3 Ground	t3 = 30um			Subst 6L		GNL
125 u	m	er3 = 4.2	H3 = 125um + t4 => H3 = 155um	Er[1]=er1 H H[1]=H1 T	[6]=H6 [6]=t6	GN
 L4 Signal	t4 = + 30um			I[1]=t1 E Fr[2]=er2 H	:r[/]=er/ {[7]=H7	
		er4 = 4.2	H4 = 600 um	H[2]=H2 T T[2]=t2 T	[7]=t7 [8]=t8	
L5 Signal	t5 = - 30um	er5 = 4.2	H5 = H3 = 155um	Er[3]=er3 L H[3]=H3 L	ayerType[1]=blank ayerType[2]=signal	
125 um				T[3]=t3 L Er[4]=er4 L	LayerType[3]=ground LayerType[4]=signal	
L6 Ground	t6 = 30um			H[4]=H4 L	ayerType[5]=signal	
100 u	m	er6 = 4.1	H6 = H2 = 100um	T[4]=t4 L	ayerType[6]=ground	
L7 Signal	t7 = - 43um	er7 = 3.8	H7 = H1 = 44um	H[5]=H5 L	ayerType[8]=blank	
L9 blank	+9 = _ 0um			Er[6]=or6		

I coats

Var Egn L Var Egn t1=+0 um t1=+0 um t2=+43 um GND t3=30 um t4=+30 um t5=-t4	H_Values H1=t2 + 1 um H2=100 um H3=125 um+t4 H4=600 um	er_Values er1=3.8 er2=4.1 er3=4.2 er4=4.2
GND t6=t3	H5=H3	ero=ero
t7=-t2	H6=H2	ero=er2
t8=-t1	H/=H1	er/-eri
con_tand_Values cond=5.959000e+ cond_MS=3.43000 tand=0.035	07 D0e+07	

Blue separation lines show how the different blocks of the definition belong together

Negative Thickness means metal grows down, positive metal thickness means it grows up!

2) Schematic Simulation Issue: Complex schematics



X Due to a simple Graphical User Interface even beginners can get very simple and fast simulation results

- As for all graphical programming tools this implies the risk of an uncontrolled code growth
- Example how NOT to do it:
- > Difficult to ...
 - ... understand
 - ... document
 - ... debug
 - ... transfer



2) Schematic Simulation Solution: Discipline!



 \times Use all ADS features to keep your design small and clean:

- Use Boundaries (e. g. Drawing formats) to limit the size of your circuit
- Vuse subcircuits
- > Draw meaningful symbols
- \times This stuff will cost some time, but the result is worth the effort

2) Schematic Simulation **Discipline: User Borders**



- \times The Palette "Drawing Formats" provides templates for drawing sheets.
- \times Adjust them if you don't like the appearance, but use boundaries for your circuit!
- \times How to make the "Drawing Format" selectable:





Design was not save so far, therefore some variables are empty!





2) Schematic Simulation Discipline: Use meaningful Symbols



imes Add drawing layers for Symbol drawing

Add layers from the end, don't touch the original ADS layers

Use this schematic.lay as standard layer file by saving it e.g.

ymbouyaidan				л.	- PL	ж		INCO			5 101
Poptical		-			1	1	Filled 🗸]ō	Solid		
)raw_Brown		•	-	-	1	1	Both 👻	0	Solid	•	
)raw_Grey		•	-	-	V	V	Both 👻]0	Solid	•	
)raw_Grey_Dark		•	-	-	1	1	Both 👻	0	Solid	•	
)raw_Red		-	-	-	1	1	Both 👻	0	Solid	•	
oraw_Red_Dark		•	-	•	1	1	Both 👻	0	Solid	•	
Draw_Blue		-	-	•	1	1	Both 👻	0	Solid	•	
)raw_Blue_Dark		-	-	-	1	1	Both 👻	0	Solid	•	
)raw_Pink		-	-	-	1	1	Both 👻	0	Solid	•	
)raw_Green		-	-	-	1	V	Both 👻]0	Solid	•	
)raw_Green_Dar	k 📃	-	-	-	1	1	Both 👻	0	Solid	•	
Praw_Yellow		-		•	1	1	Both 👻	0	Solid	•	
.ogo_Black_Trans	sp	-	-	-		1	Filled 👻	95	Solid	•	
.ogo_Red_Trans	oa 👘	-	-	-		1	Filled 👻	95	Solid	•	
ogo_Black		-	-	-		1	Both 👻	0	Solid	•	
ogo_Red		•	-	•		1	Both 👻	0	Solid	•	
ormat_Outline		-	-	•		1	Outline 👻	0	Solid	•	
ormat_Text		•	-	-		1	Both 👻	0	Solid	•	
Visit	ole			5	Shape	Displa	v Trans. % Lin	e Style Lay	/er		
lone	All		None			•	•		New	Cut	Paste
ssages:											
-											
Apply			Reset]		Save.		Read	Cance		Help



2) Schematic Simulation Discipline: Arrangement of Circuit



imes Use only symbols with the same pitch



2) Schematic Simulation Discipline: Arrangement of Circuit



X Advantage: Simplifies the work for ADS automatic rewiring when shifting components!





2) Schematic Simulation Discipline: Arrangement of Circuit



 \times Advantage: Connecting components faster



2) Schematic Simulation

Discipline: Give only important information

- \times Hide not required information
- \times Give meaningful instance names



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3) 3D EM ML for Momentum When to use this tool ?

Some structures can not be modeled with the Multilayer transmission line library

- If you need to simulate a structure with a Slot in the Reference plane the 3D Multilayer EM Field solver for Momentum is the tool of choice
- ✓ Usually such existing Layouts are too complicated to be Re-drawn. In this case it is required to transfer the Layout from the Layout tool to ADS Layout.
 - For Cadence Allegro there is a very good interface available: The Allegro DFI (Design Flow Integration)

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3) 3D EM ML for Momentum Problem Description

 \times In order to reduce layers an asymmetric stripline concept was chosen for an embedded board layout

- On one side a good GND referencing was given in close proximity, while on the other side a splitted power plane in further distance was implemented.
- \times Target of investigation:
 - Do a check if the non ideal power referencing is causing any Problems!



Routing over a split in the second Reference



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3) 3D EM ML for Momentum Problem Description

- EVE KNOW HOW HIGH SPEED SIMULATION AND MEASUREMENT
- X This is an example where we extracted the S-Parameter for a CA bus on an embedded computer module.
- imes The board area was about 3x3 inches
- \times Signals included: 2x CLK, 4x CA signals
 - Connecting to 8 DRAMs, one controller and some Terminations this results in 62 ports!

3) 3D EM ML for Momentum Prerequisites for the Allegro DFI



 \times The DFI consists of two parts:

- ✓ The Interface in Allegro
- The Allegro import Design kit in Momentum

 \times Preparation

- Install the DFI in Allegro according to the help
- Install the Allegro import Design Kit in ADS
- Think about your requirements!
 - If you need a big layout you need to focus on model size reduction and reduce your accuracy settings
 - If you need an accurate high speed model you need to take a mall part of the layout with high accuracy settings

1) Trace Select 2) Layer Select 3) Cookie Cutter 4) Component/Pin Select 5) Po Autoplace Ports Clear Clear all existing ports	ats
AutoPlace Create ports for the selected pins V Do not add negative ref. p	ains
Port List	
B ✓ Port 001 : CLK1+.R21 B ✓ Port 002 : CLK1+.U222 B ✓ Port 002 : CLK1U221 B ✓ Port 005 : CLK1U223 B ✓ Port 007 : CLK2+.R3.1 B ✓ Port 008 : CLK2+.U226 B ✓ Port 009 : CLK2U23.14 B ✓ Port 010 : CLK2R3.2 B ✓ Port 010 : CLK2R3.2 B ✓ Port 010 : CLK2U3.15 B ✓ Port 010 : CLK2U3.15 B ✓ Port 011 : CLK2U2.3.15 B ✓ Port 013 : CLK3U3.15 B ✓ Port 013 : CLK3U3.26 B ✓ Port 016 : CLK3U3.6 B ✓ Port 016 : CLK3R4.2 Add Delete Edt	
Verify ports Verify/Update Port verification and (re)numbering: NotNeeded 11 Traces Ready 21 Contex Ready 51 Ports Ready 21 Layers Ready 41 Component/Pris Ready OK OK	Cancel

3) 3D EM ML for Momentum The Allegro DFI interface

 \times The accuracy settings for Allegro DFI are defined in the eemom.option file

If a design specific file is used it needs to be in the same directory as the design and called "Designname.eemom"

For the described problem a reduced accuracy was required to reduce the model size.

 \checkmark Vias and pads can be exported as squares

- ARC resolution can be reduced
- GND holes could be skipped, but this was done during the simplification in ADS

Imported Layout Only signal layers **EYE KNOW HOW**

3) 3D EM ML for Momentum Simplification in Momentum

imes To get a reasonable model size the layout needs some further simplification in Momentum

- Convert Strip to Slot supply layers
- Remove not required vias
- Remove not required openings in Supply layers
- > Delete not required metal on Signal layers

Simplified Layout Only signal layers **EYE KNOW HOW**

3) 3D EM ML for Momentum Connectivity check in Momentum



➤ During Simplification it is possible to delete something that is still needed → Often check the connectivity!

- Several connectivity checks are implemented in Momentum
- A fast and easy check is available under "Allegro Tools → Allegro Nets!
 - This can have problems with routing on slot layers



3) 3D EM ML for Momentum

Preprocessing and Settings in Momentum

 \times Further methods to reduce simulation time

- Preprocessing with "Layout Healing", "Shape Merging" and "Layout simplification" enabled
- Meshing and Simulation settings
 - Enable Edge Mesh only for signal layers using layer based settings

	Global Layer Primitive Primitive Seed Define here the mesh values for the entire circuit	Mesh Setup Controls:1 Global Layer Primitive Primitive Seed Define here the values that apply to a specific layer	
	Preprocessor settings Mesh Frequency 2 GHz • Mesh Density 20 cells/wavelength Arc Resolution (max. 45 deg) 45 degrees Edge Mesh Edge Width (leave empty	Layout Layers TCH_TOP	
	or 0 for automatic size) U mm V Transmission Line Mesh Number of Cells Wide 0	Mesh Density 20 cells/wavelength	
Global Mesh settings	Thin layer overlap extraction Mesh reduction Horizontal side currents (thick conductors)	or 0 for automatic size) 0 mm v Transmission Line Mesh Number of Cells Wide 3	Layer based Mesh settings
	OK Reset Clear Cancel Help	OK Reset Clear Cancel Help	

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4) Data Evaluation Simulation Results: Multilayer T-Lines



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4) Data Evaluation Simulation Results: S-Parameter





4) Data Evaluation DDR2/DDR3 Design Kit



 \times Another option to evaluate DDR2/DDR3 simulations are

	Se la constante de la constant	Ħ	## <u>Pero</u>	ML>	
Datasets and Equations			Traces		
_CLK_MA6_t1_533_1ps_withDerating	•		Tra	ace Options	
Search	4	st 💌	CmdAdd_ClockSkew	SetupRise.MA6_t1	enue
ClockFlightTimeFall.CLK_t1			CmdAdd_ClockSkew	SetupFall.MA6_t1	1.1.1
ClockFlightTimeRise.CLK_t1			CmdAdd_ClockSkew	Holdfüse.MAb_t1	
ClockSlewRFall.CLK_t1			CmdAdd_ClockSkew	HoldFallMAb_tL	
ClockSlewRRise.CLK_t1	1	>>Add >>			2
ClockVIX.CLK_t1					
CmdAdd_ClockSkewHoldFall.MA6_t1					
CmdAdd_ClockSkewHoldRise.MA6_t1					
CmdAdd_ClockSkewSetupFall.MA6_t1					
CmdAdd_ClockSkewSetupRise.MA6_t1		>Add Vs>>			
CmdAddFlightTimeHoldFall.MA6_t1					
CmdAddFlightTimeHoldRise.MA6_t1					
CmdAddFlightTimeSetupFall.MA6_t1	5				
CmdAddFlightTimeSetupRise.MA6_t1					
CmdAddNoiseMarginHigh.MA0_t1		<< Delete <<			
CmdAddNoiseMarginLow/MA6_tL					
CmdAddOvershootArea MA6 4 Feil					
CmdAddOvershootArea MA6 t1 Pass					
CmdAddOvershootPeak MA6 t1	-				
CmdAddOvershootPeak.MA6 t1.Fail					
CmdAddOvershootPeak.MA6 t1.Pass					
CmdAddSlewRHoldFalLMA6 t1					
CmdAddSlewRHoldRise.MA6_t1	1	ariable Info			
CmdAddSlewRSetupFall.MA6_t1					
CmdAddSlewRSetupRise.MA6_t1					
CmdAddUndershootArea.MA6_t1					
CmdAddUndershootArea.MA6_t1.Fail		Manager			
CmdAddUndershootArea.MA6_t1.Pass		manage			
CmdAddUndershootPeak.MA6_t1					
CmdAddUndershootPeak.MA6_t1.Fail					and the second
CmdAddUndershootPeak.MA6_t1.Pass	-				to
Enter any Equation		>> Add >>			

Index	etupRise.MA6_t1	SetupFall.MA6_t1	HoldRise.MA6_t1	HoldFall.MA6_t1
1.000	322.505	310,636	-55.132	-49.349
2.000	321.481	311,025	-56.010	-50.362
3.000	322.991	364,654	-110.759	-74.597
5.000	530.344	363,308	-73.709	-72.568
5.000	398.833	362,338	-117.505	-72.284
6.000	533.291	424,338	-116.248	-106.536
7.000	532.599	422,272	-75.610	-102.234

4) Data Evaluation DDR2/DDR3 Design Kit



 \times With the Excel Report a nice report file is written

File Edit Select View Insert	Options Tools Layout Simulate Window D Options Tools Layout Simulate Sim	ynamicLink EKH Menue Design Control to the second sec	Koui F (
rement	Signal	Minimum	Maximum	Average
d_ClockSkewSetupFall	MA6_t1	310,6360812	424,3375578	365,5100146
d_ClockSkewSetupRise	MA6_t1	321,4806629	533,2914575	423,1491912
d_ClockSkewHoldFall	MA6_t1	-106,5358198	-49,34885743	-75,41849373
d_ClockSkewHoldRise	MA6_t1	-117,5047894	-55,1315254	-86,42465638

4) Data Evaluation DDR2 Design Kit: Eye Opening

 \times EKH Eye calculations:

- Valid Window: 3.15ns (includes Clock skew)
- \checkmark Setup+Hold = 3.09ns (no clock skew)

 \times DDR2 Design Kit calculation

Eye opening from AC crossing to DC crossing:
 UI – (max skewSetup – min skew hold)
 3750p – (533.3ps – (-117.5p)) = 3099.2ps

\times Difference:

- Design kit is cycle based (and more accurate)
- KH calculation is Eye based (and a bit overcritical)

Measurement	Signal	Minimum	Maximum	Average
CmdAdd_ClockSkewSetupFall	MA6_t1	310,6360812	424,3375578	365,5100146
CmdAdd_ClockSkewSetupRise	MA6_t1	321,4806629	533,2914575	423,1491912
CmdAdd_ClockSkewHoldFall	MA6_t1	-106,5358198	-49,34885743	-75,41849373
CmdAdd_ClockSkewHoldRise	MA6_t1	-117,5047894	-55,1315254	-86,42465638

DDR2 Design Kit results



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EKH Calculation

indep(caltst1)	caltst1
Setup time [0]	2,743 n
Hold time [1]	347.6 p
Diff Clock skew [2]	58.66 p
Valid window [3]	3,149 n
CLK skew start[4]	1,836 n
CLK skew end[5]	1,896 n
Valid window start[7]	2,243 n
Valid window start[7]	-906.4 p
Delay[8]	3,062 n
vret[9]	900.0 m

4) Data Evaluation **Using Templates and Predefined Equations**

ADB Plot Traces & Attributes		? ×		
Plot Type Plot Options		123 4 567 8	Plot Type	
ADS UserGroup Simulation		Trace Options	Datasets	and Eq
	[1:-t		Predefine	ed Equ
ZZZ_Designer_Company ZZZ_Designer_email ZZZ_Designer_name ZZZ_Designer_phone ZZZ_Designer_Website ZZZ_my_data_dir ZZZ_my_design_name ZZZ_my_design_path ZZZ_my_formated_sim_datetime ZZZ_my_home_dir ZZZ_my_sim_datetime ZZZ_my_sim_datetime ZZZ_my_Sim_daterime ZZZ_my_Sim_daterime ZZZ_my_Sim_daterime	>>Add >> >>Add Vs>> << Delete << Variable Info		DDS_Fil DDS_Fil DDS_Fil DDS_Fil DDS_Fil DDS_Fil DDS_Fil Default, Default, Default, Default, Default, Default, Default,	e_van e_Path e_Size e_Crea e_Crea e_Moo e_Moo _Datas _Datas _Datas _Datas
Enter any Equation	>> Add >>			
	ncel	Help	Pre	de
Variables from De	sign		Defa	au
			Proje F:/Daten/E KH/ADS/ADS_User_Gri	et Din oup_M
Hem ann Ruckerbauer EyeknowHow ketbauer@EyeKnowHowde wwwEyeKnowHowcom +49 (0)9938 902083			ADS_UserGroup_Sin	Design nulatio

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Default Dataset Name ADS_UserGroup_Simulation.ds Current time Simulate ed Sep 01, 2010 12:40:54 Wed Sep 01, 2010 12:42:



4) Data Evaluation Use Tabs



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4) Data Evaluation Manual Table Format

Proj	ect Directory	/Daten/EKH/AD	S/Agilent_CA_Simulation	n_Momentum	_prj Design Name	.dsn	CAS_Extracted Default Dataset	l_2Ghz_inclAggreds t Name
	rate UI		Ove	rview	Table			
Agilent	Plot Traces & Attributes		? 🗾					
	Plat Type Plat Online							
	Plot Type Plot Options							
			5673					
	Datasets and Equations		Traces					
	Equations	-	Trace Options					
	Search	List 👻	plot_vs(Values_Sig1, Value_names)					
	UI_Sig3		plot_vs(Values_Sig2, Value_names)			ADS LIST T	ormat	
	UI_Sig4	>>Add >>				ISI ne Sig1	tRX ps Sig2	tRX ns Sig1
	Value_names	>>Add Vs>>			133.917	125,936	2330.778	2341.522
	Value_names1							
	Values_Sig1 Values Sig1a	<< Delete <<						
	Values_Sig2	L						
	Values_Sig2a	Variable Info						
	Values_Sig3 Values_Sig4	variable info						
	a0	Manage						
	al	*						
	Enter any Equation	>> Add >>						
	OK	Cancel	Help					
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	Hermann Ruckerbauer						Curre	ant time
herma	ann.ruckerbauer@EyeKnowHow.de							
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5) 3D FEM Simulation When to use this tool ?



- We have seen a Momentum simulation of a large PCB with reduced accuracy in order to get the simulation done.
- \times If the signal rates require a high accuracy then the 3D EM FEM field solver is the tool of choice
 - \nearrow This gives a high level of accuracy, but
 - This can only handle small structures
- \times Predestinated usage for the 3D EM FEM tool:
 - ✓ Bond wires in a package
 - \checkmark Vias on a PCB or in Silicon
- \times Following the optimization of a differential via for 10Gb data rates

5) 3D FEM Simulation Problem Description



- X Target of the investigation was to optimize a Via based on an existing stackup for 100 Ohm differential Impedance.
- X Data source was a Layout exported as ODB++ that was imported into ADS Layout.
 - Strong recommendation is to re-draw the structure and NOT to use the imported data for simulation
 - Advantages of Re-Drawing
 - Dimensions are accurate what simplifies simulation and reduces simulation time (more important than you might think ...)
 - Changes are simpler as circles are Circles and not just polygons. By this it is vey easy to change e.g. the radius of a cutout

5) 3D FEM Simulation Two Basic configurations



\times Double Stich GND



 \times Single Stich GND

 \times Parameters for Optimization

- **Number of stitch vias**
- Distance of stitch vias
- ✓ Size of plane cutouts
- **Via pads and antipads**

5) 3D FEM Simulation Tasks for Preparation: Port Definition

 \times As in the 2.5D simulation: One of the most difficult things is the correct definition of the ports in the setup

 \sim In the Momentum example "internal" ports have been used \sim In this example "single" ports are used

		A				
Port 1 selected on STRIP layer layer_1 .		<u> </u>				
Port Type	S-parame	ter Ports		_		
Single Made	Numbe	r Name	Ref Impedance	Туре	Ref Offset [i	
Single Mode		l Term1	50 + 0j	Single Mode	0	
Polarity		2 lerm2	50 + 0j	Single Mode	0	
Normal Reversed		s ierms I Term/	50 + 0j 50 + 0j	Single Mode	0	
Impedance		+ ICIII+	50 + 0j	Single Mode	Ŭ	
Real						
50 Ohm	-					
O Obm	- Lavout P	orts				
Cim	Numbe	r Name	Connected to	Laver	X [um]	
Reference Offset (+ = inward)		P1 Sig top	+ Term1	laver 1	-950	
0 um	•	P2 Sig 13	 Term2 	laver 16	950	
Associate with port number	Q+ 3	P3 Sigb top	+ Term3	layer 1	-950	
		P4_Sigb_L3	+ Term4	layer_16	950	
Port Info						
Single Mode STRIP port						
- extended calibration	•				•	
	Auto	select 🔽 Auto center	Auto zoom			Dort Viou
l						For viewe
OK Apply Cancel	Help			Close	Help	

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5) 3D FEM Simulation

Tasks for Preparation: Substrate definition

Momentum and FEM Substrate are very similar (and using the same basis)

- Slight difference is the support of dielectric vias (e. g. for solderstop openings)
- The definition of the Multilayer Transmissionline substrate definition is different to Momentum
- X Always verify dimensions in the 3D viewer with the measurement tool!



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5) 3D FEM Simulation Final Via Definition



 \times In a first step the optimization was done with Momentum and the "3D Distributed" via model in the stackup!

- \nearrow This is a reasonable approach for a fast optimization
- The final model was generated using the 3D FEM solver!
- X After optimizing the dimensions we found still some possible improvements:
 - Shortly before the via the differential routing gets wider and the impedance increases
 - To compensate this the cutout on top and bottom was reduced
 - Sut overall the via is capacitive
 - To improve this we removed the Pads on the center Supply layers





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6) FrontPanel routines Via Evaluation: SP-TDR



X The via parasitics have been evaluated with the FrontPanel SP-TDR

This routine calculates a TDR based on S-Parameters

\times Settings used for Data evaluation

- > Define structure as Differential ("Frequency Modes")
- \sim Do the evaluation from 0 to 500ps ("Transform Sweep (Time)")
- Velocity to 0.5 * 3e8 m/s ("Global Parameters")

Delay of 1.5cm ("Port Extension")

Slight "Hamming window with a = 0.9 ("Window")

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PEEL

1Av?

SWEEP

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99

98

0.0000

mpedance



100.0p

200.0p

time, sec

300.0p

400.0p

500.0p

Reduction of this peak was possible by reducing C due via pad removal at center supply pads!

6) FrontPanel routines FP-Eye

The FP-Eye routine in the Data Display is a good way to get a fast display of a dataeye without knowing any equations

- Disadvantage is the handling:
 - Scaling of the Window
 - Difficult documentation
 - Only single eye is displayed
 - Fixed number format

Mode Select Dataset Select Trace Okoloscope Konton, MUX, ModTX, CarrRX, v01 Diffout Pre/Mask Diffout Diffout Image: Select Dataset Select Trace Image: Select Dataset <	
Node Octoberspop De Dye Mask Select Dataset Dentrom, MAX, ModDy, CorrRX, v01 Select Trace Image: Description of the Description of t	Measurement Settings
Indiana Select Dataset Select Trace Decisions Decisions Decisions Select Dataset Select Trace Decisions Decisions Decisions Decisions Decisions De	Data Type = NRZ Start Time = 2.840753111e-008 Storp Time = 50-007 Data Rate = 500000000 Top-Base Definition = "Auto" Threshold=nation = "Auto" Threshold=20 - 80% Eye Boundary =40 - 60%
Occidescope Entron MUK_ModX_CamRX_v01 • Diffut Exceloration Diffut Messurements Entron MUK_ModX_CamRX_v01 • Diffut Image: A comparements	
Eve/Mak Dataset: Konton, NUX, Modrix, Carrist, VP1 Image: Status and Statu	-
4:5-	Measurement Results Eye Level Zero -0.49472067601 Fye Level One -0.07430464555 Fye Level Mean -0.28451716078 Fye Amplitude 0.4204259304669 Fye Hypitrude 0.4204259304659
time, page Color Grade	450 Eye Height (db) -5.9642216172515
	Eye Width 1.0/36347e-010
	Eye Opening Fa 0.380000024222303
	Eye Signal_to_N 7.1704450701510
	Eye Duty Cycle 0.9886-013
	Eye Duty Cycle 0.34940213678384
	Eye Kise Time 1.0102205e-010
	Eye Fall Time 9.915671e-011
	Eye Jitter (PP) 3.192286e-011

EYF KNOW HOW

Normally we use the FP-Eye with the "Save as normal .dds" as basis for own evaluation sheets!



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2) Analog/RF Schematic Simulations

3) 3D Multilayer EM for Momentum

4) Data evaluation with the Data Display

5) Arbitrary 3DEM for FEM and FDTD Elements in EMPro and ADS

6) FrontPanel routines

7) Conclusion

8) Backup



imes This was just a small overview how to use ADS for SI

- There are many other parts of ADS that have not been touched
 - The digital Ptolemy system simulator
 - Model support (e. g. IBIS)
 - ... and a lot more
- Additionally a lot of interfaces to other tools and models are available
 - Matlab, HSPICE, ..
 - IBIS-AMI, X-Parameter, …
 - Hardware …
 - ... and a lot more



ADS is the Swiss army knife of EDA!



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4) Data Evaluation DDR2 Design Kit: Clock delay

 \times To simulate the correct Crosstalk the clock needs to be delayed by around 0.5 tck.

- \times But this does is not the perfect adjustment to get symmetric setup and hold margins.
- \times It is difficult, but possible to calculate the perfect clock delay out of the measurements from the DDR2 Design kit
- \times This clock delay can be used to calculate setup /hold times for the DRAM

FYF KNOW

4) Data Evaluation DDR2 Design Kit: Clock delay

 \times Add DRAM tSH to skew:

- \checkmark Max SetupSkew + tsetup = 512ps + 250 ps = 762ps
- \checkmark Min Holdskew thold = -94ps 375ps = -469 ps
- imes A delay of 2.02ns would place the clock perfectly
 - Need to add the flight time difference between CLK and CA!
 - This was calculated based on Slew Rate, Flight Time Clock and Flight time CA to 185ps
 20
 - Or can be simulated …
 - A 2.2ns delay was added to the CLK

Probe	Measurement	Signal	Minimum	Maximum	Average
MA6_t1	CmdAdd_ClockSkewSetupFall	MA6_t1	395,1531007	449,6923219	425,9007699
MA6_t1	CmdAdd_ClockSkewSetupRise	MA6_t1	396,6127588	512,82657	448,8582792
MA6_t1	CmdAdd_ClockSkewHoldFall	MA6_t1	-79,7608975	-3,208134984	-45,58591197
MA6_t1	CmdAdd_ClockSkewHoldRise	MA6_t1	-94,28593739	-8,268098824	-56,13336704



FYF KNOW

Setup/Hold @ 533

tSetup = 250p

tHold= 375p

4) Data Evaluation DDR2 Design Kit: Clock delay

EKH Eye Calculation (tSH not considered in Measurement)

- Setup Margin: 1.469 0.250 = 1.219
- \checkmark Hold Margin: 1.581 0.375 = 1.206



 \times For a final Timing Budget calculation there is only missing the information on Controller output timings

EYF KNOW HOW