EKH - EyeKnowHow

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

ADS User Group Meeting
Sept. 28th 2010
Andover (MA)

Agenda

EYE KNOW HOW
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1) Introduction

2) Analog/RF Schematic Simulations

3) 3D Multilayer EM for Momentum

4) Data evaluation with the Data Display

5) Arbitrary 3DEM for FEM and FDTD Elements in EMPro and ADS

6) FrontPanel routines

7) Conclusion

8) Backup

1) Introduction
ADS: The Swiss army knife of EDA

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- "Signal Integrity" (SI) covers a wide range of topics!
- There are a lot of different tools out that cover parts of the topics included in SI. Using different tools means:
  - Learn new handling for each tool!
  - A lot of Import/Export tasks are required!
- EKH uses ADS as single solution for all signal integrity related investigations.
  - Memory interfaces (e. g. DDR2 / DDR3 …)
  - High speed interfaces (e. g. PCIe, 10Gb Ethernet...)

- This presentation gives an overview how we use ADS combined with some of our Tips and Tricks!

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2) Schematic Simulation
The Multilayer Transmission line Library

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- Schematic based simulation can often replace layout based simulations
- EKH does many simulations based on the Multilayer transmission line library.
  - Even “Post-Layout” simulations are done by rebuilding the topology with this models
  - Good engineering judgment is required to implement an accurate representation of the layout
    - Selecting “representative / mean” values for Spacing / Length
    - Does the Transmission line model cover the behavior of the real Layout (e. g. slots in reference planes)?

2) Schematic Simulation

The Multilayer Transmission line Library

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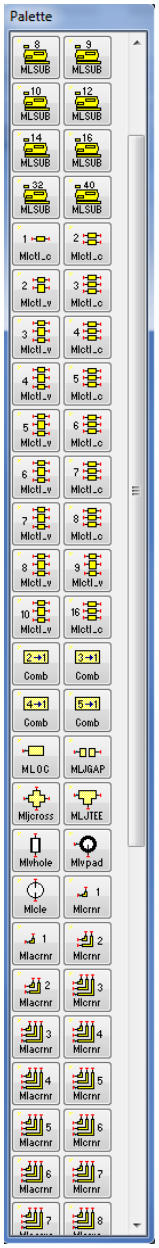


Substrates

T-Lines

Couplings

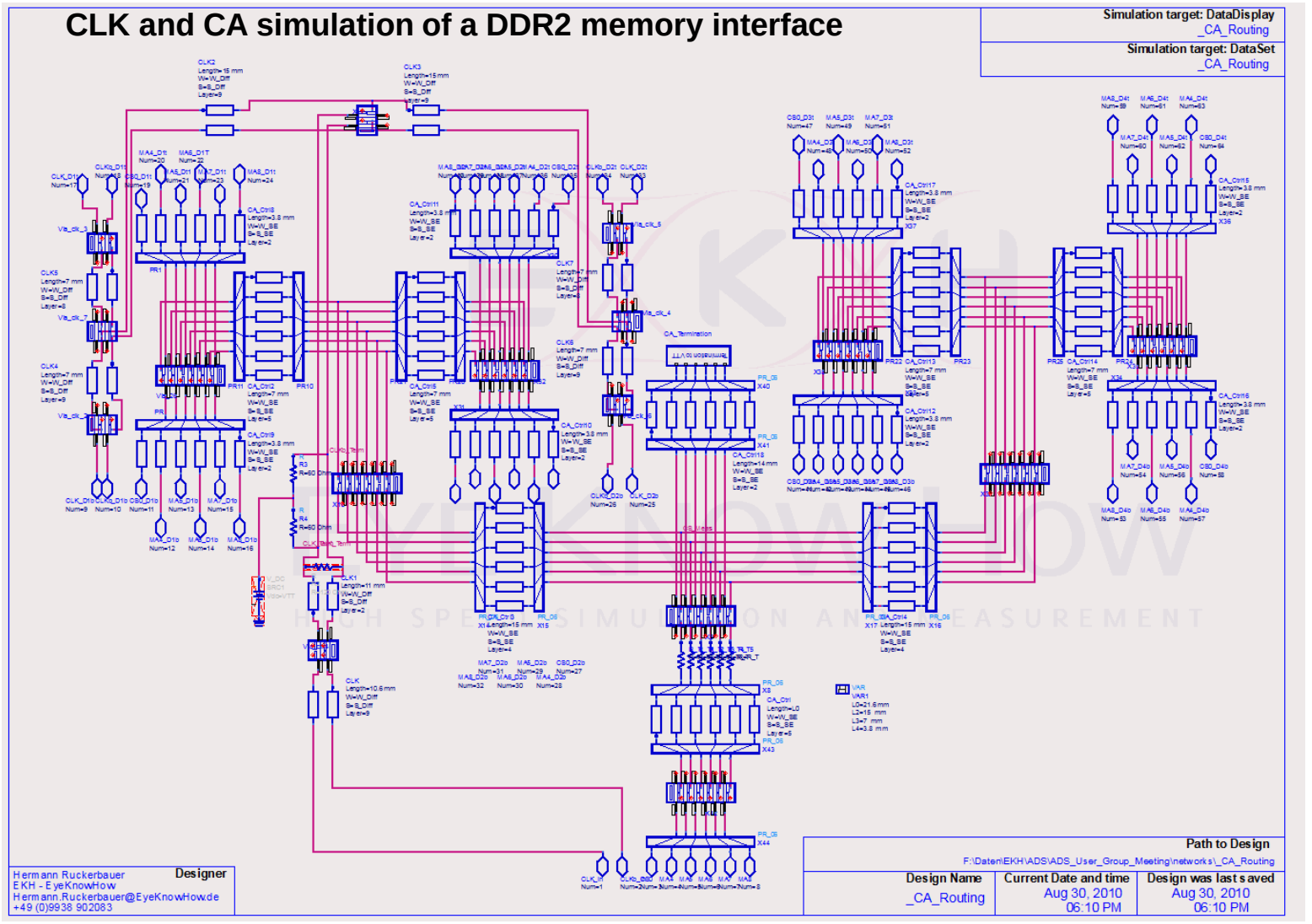
T Structures

Vias

Bends

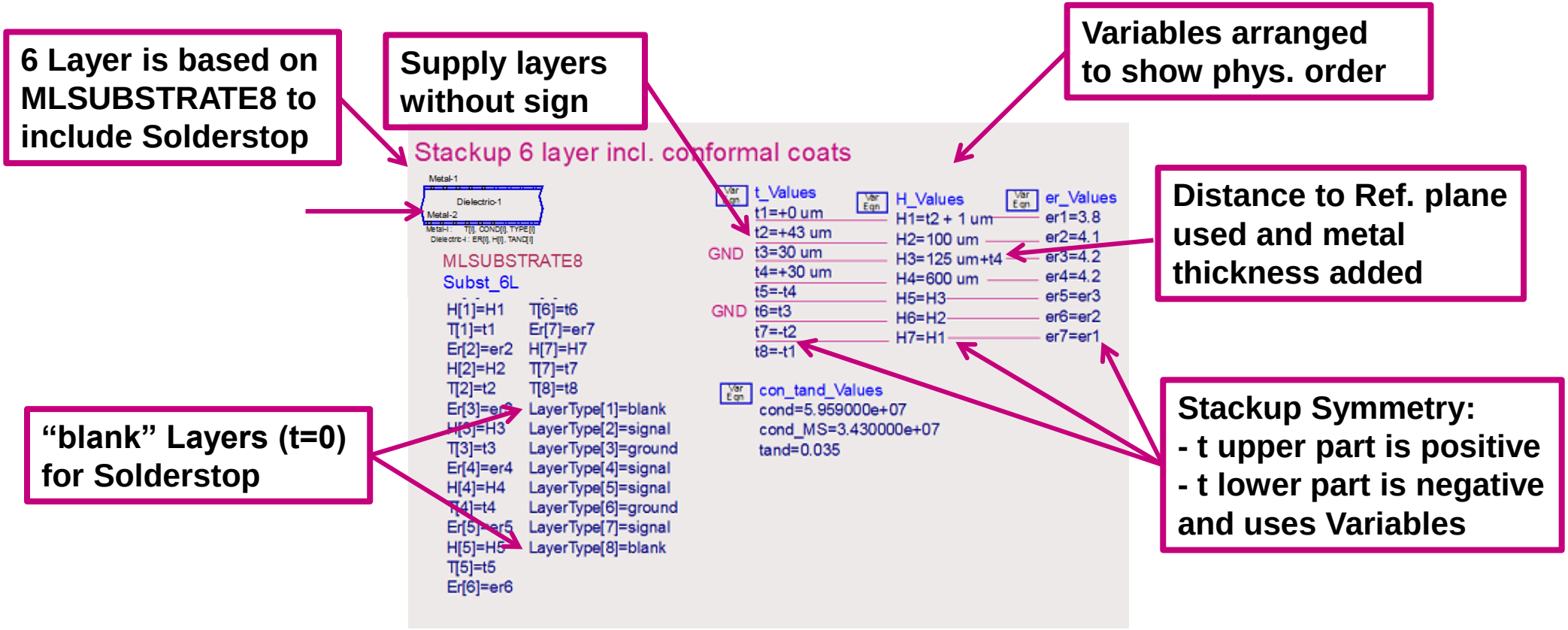
…

and much more



2) Schematic Simulation
Stackup definition

- Stackup definition is not that simple, so we generated some templates to simplify the process.



- **Once the Stackup is defined all variables will be hidden**

2) Schematic Simulation
Stackup definition

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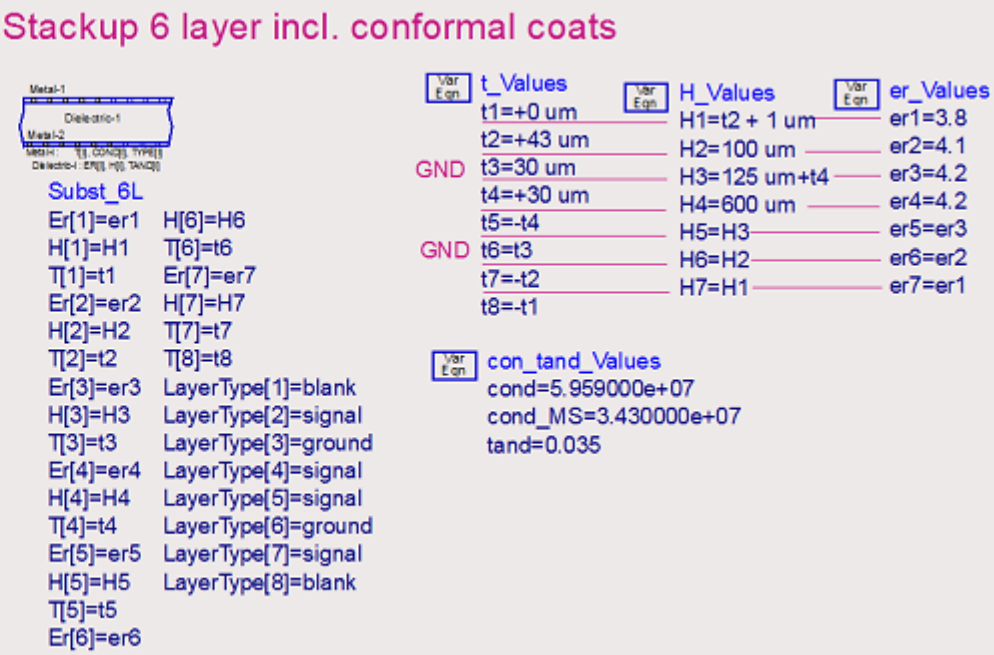
- Physical view of the Stackup
  - Physical view is drawn in ADS on additional layers

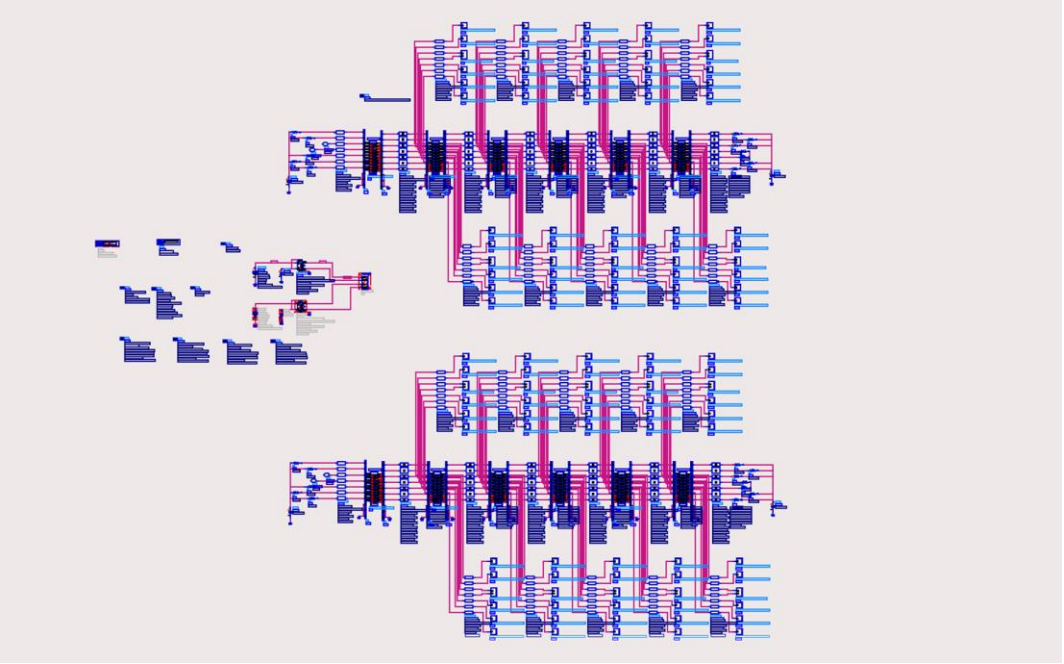


Blue separation lines show how the different blocks of the definition belong together

Negative Thickness means metal grows down, positive metal thickness means it grows up!

2) Schematic Simulation
Issue: Complex schematics

- Due to a simple Graphical User Interface even beginners can get very simple and fast simulation results
  - As for all graphical programming tools this implies the risk of an uncontrolled code growth
  - Example how NOT to do it:



  - Difficult to ...
    - ... understand
    - ... document
    - … debug
    - … transfer

2) Schematic Simulation
Solution: Discipline!

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- Use all ADS features to keep your design small and clean:
  - Use Boundaries (e. g. Drawing formats) to limit the size of your circuit
  - Use subcircuits
  - Draw meaningful symbols
  - Hide unnecessary information (e. g. component name)
- This stuff will cost some time, but the result is worth the effort

2) Schematic Simulation
Discipline: User Borders

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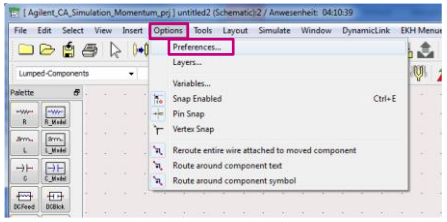
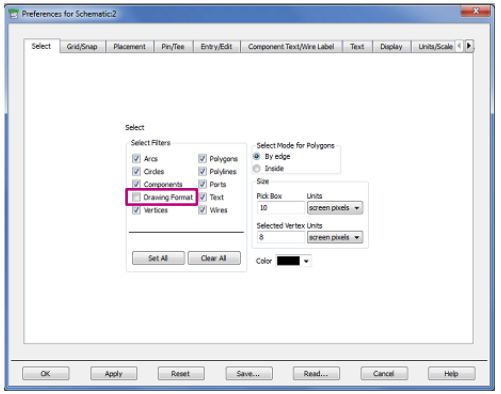
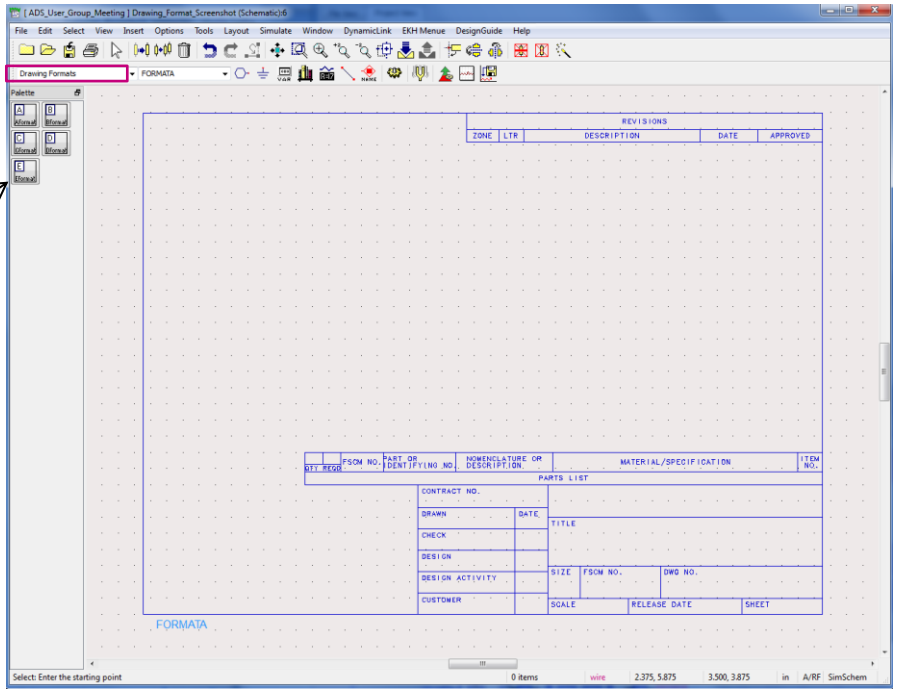
- The Palette “Drawing Formats” provides templates for drawing sheets.
- Adjust them if you don't like the appearance, but use boundaries for your circuit!
- How to make the “Drawing Format” selectable:





Palette: Drawing Format

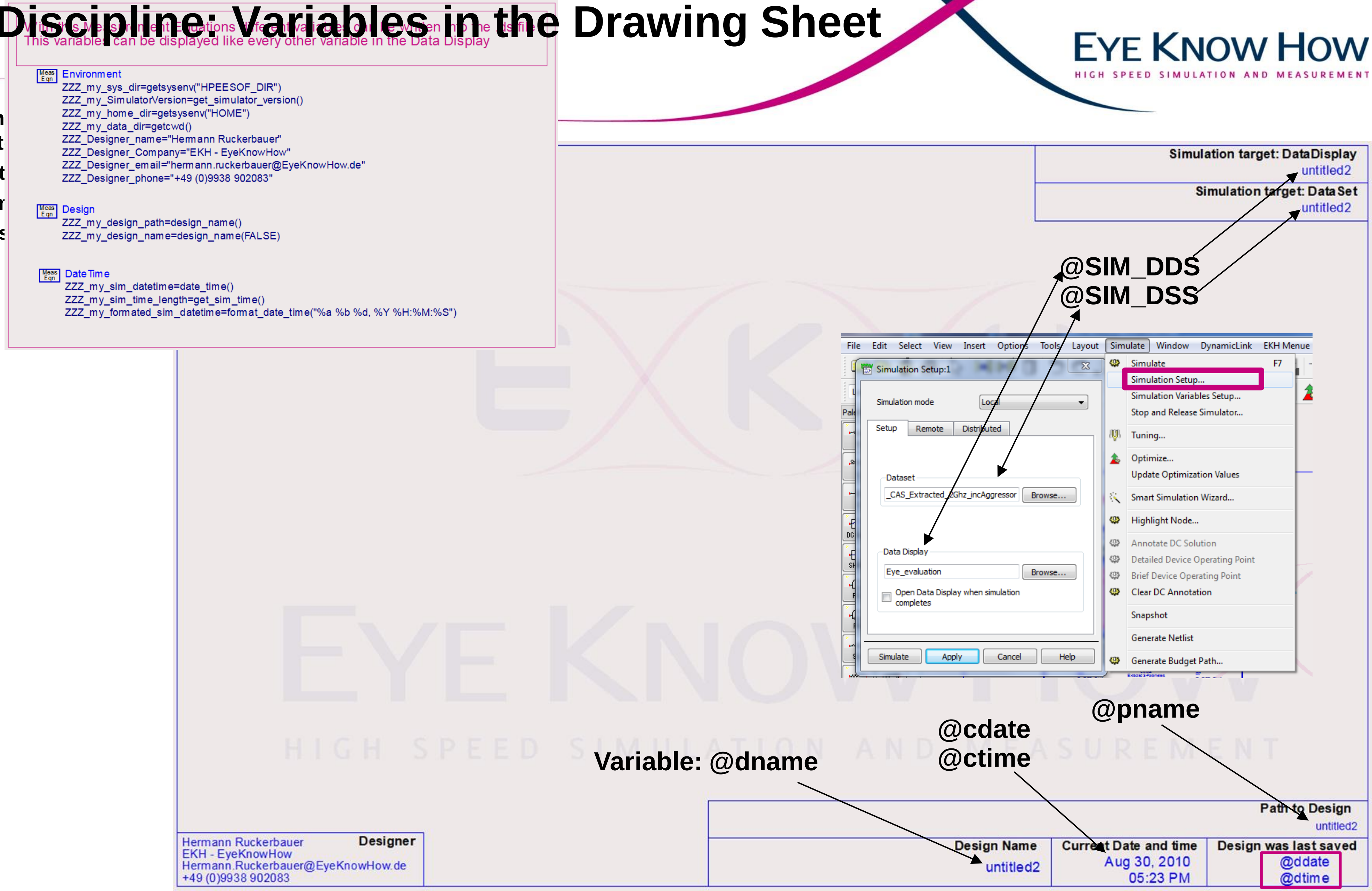


2) Schematic Simulation

Discipline: Variables in the Drawing Sheet

Som... writt...

- Dat...
- Sim...
- Des...
- …



Design was not save so far, therefore some variables are empty!

2) Schematic Simulation

Discipline: User Subcircuits

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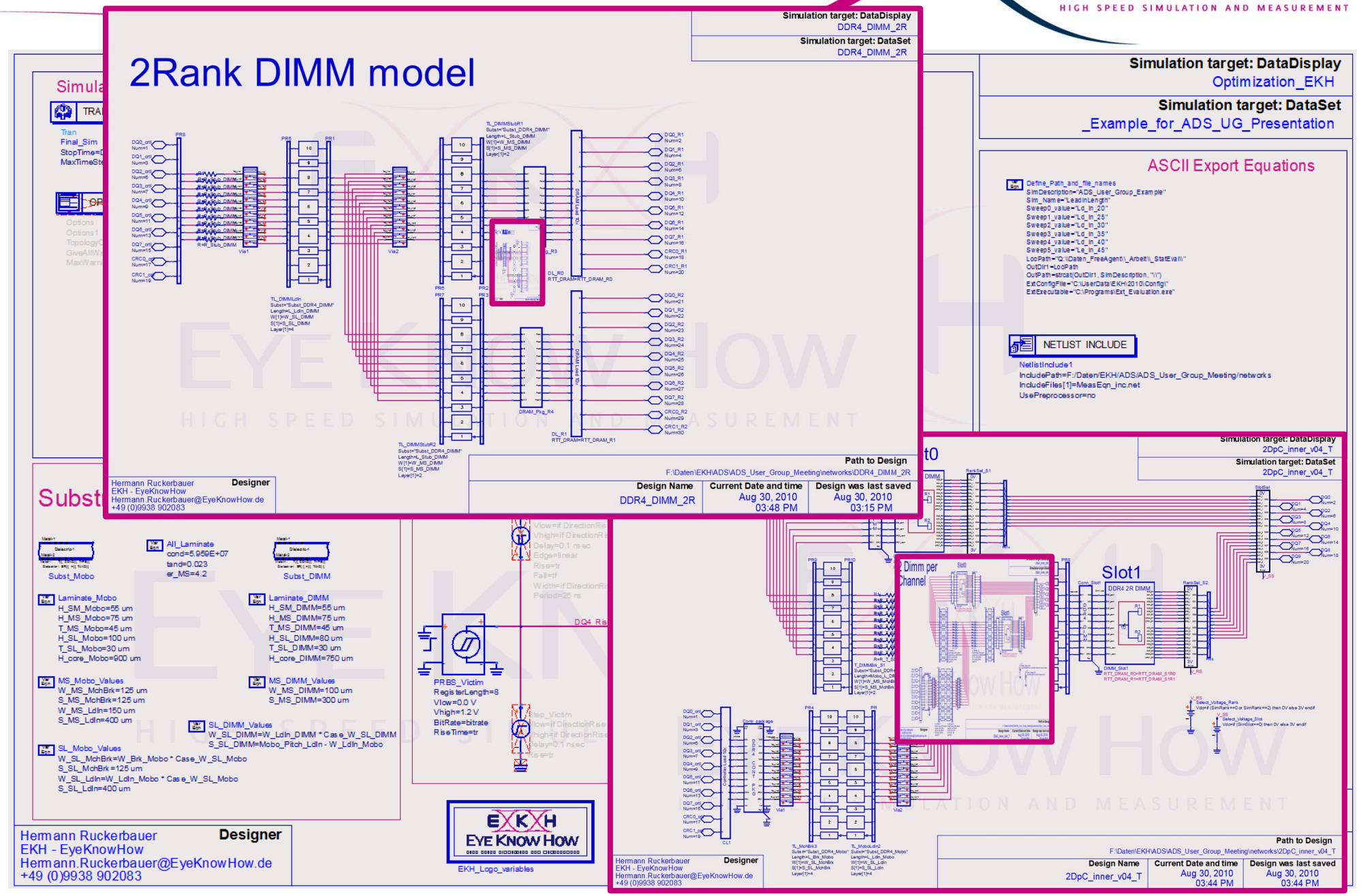
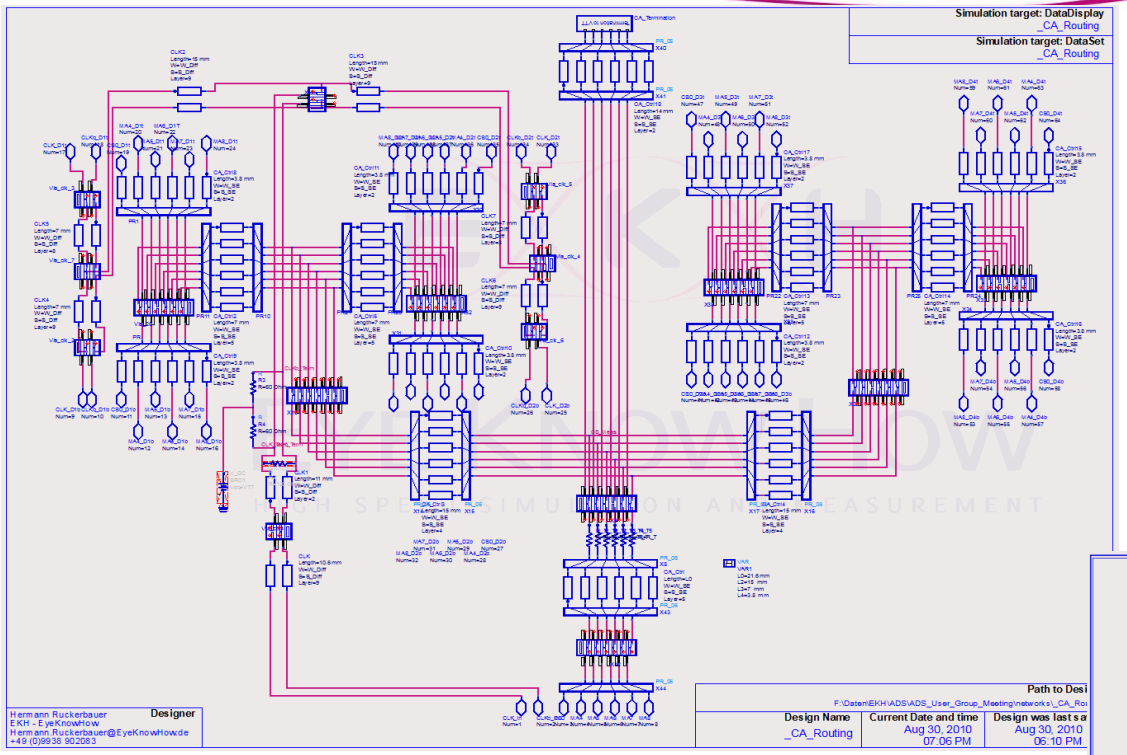
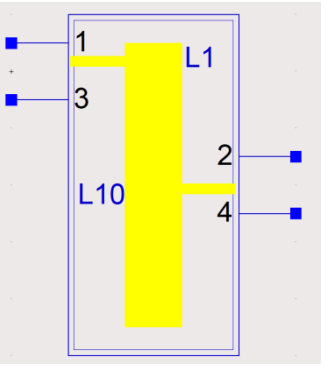


2) Schematic Simulation
Discipline: Use meaningful Symbols

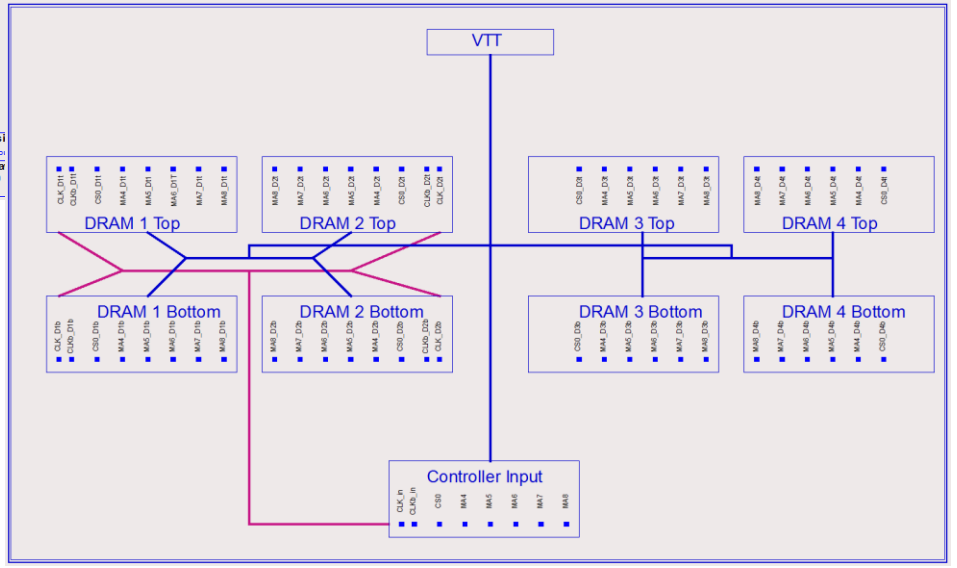


Subcircuit Schematic

Symbol for via with stub

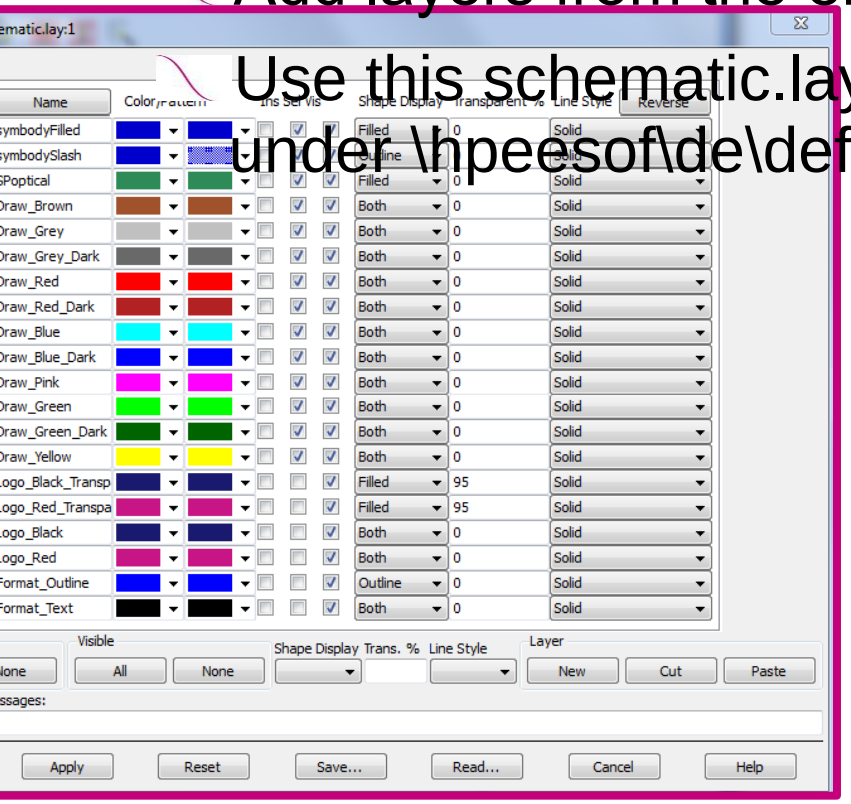


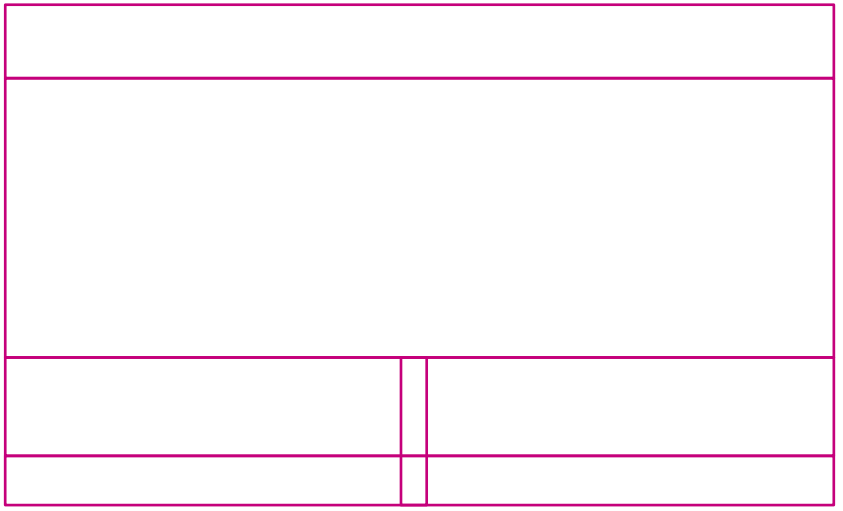
Subcircuit Symbol



2) Schematic Simulation
Discipline: Use meaningful Symbols

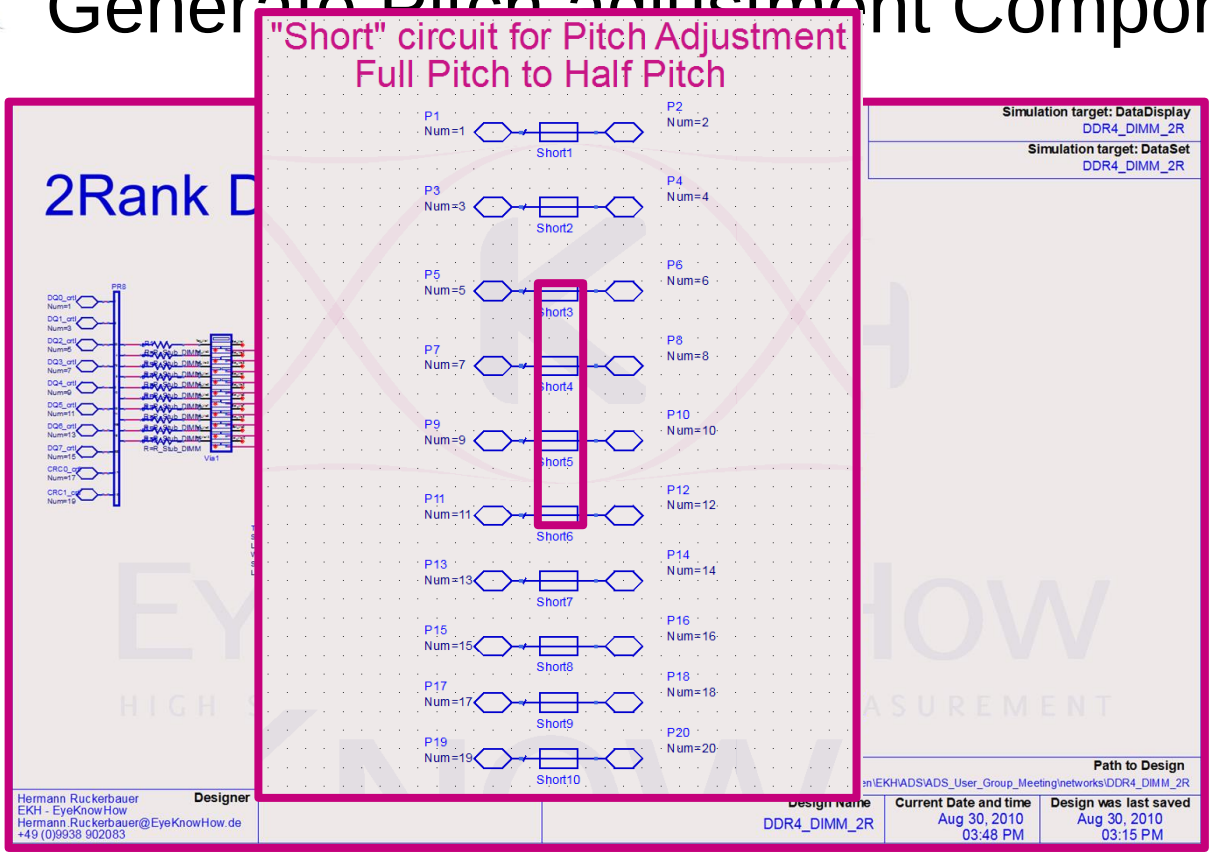
- Add drawing layers for Symbol drawing
  - Add layers from the end, don't touch the original ADS layers
  - Use this schematic.lay as standard layer file by saving it e. g. under \hpeesof\de\defaults\schematic.lay





2) Schematic Simulation
Discipline: Arrangement of Circuit

- Use only symbols with the same pitch
- Generate Pitch adjustment Components



2) Schematic Simulation
Discipline: Arrangement of Circuit

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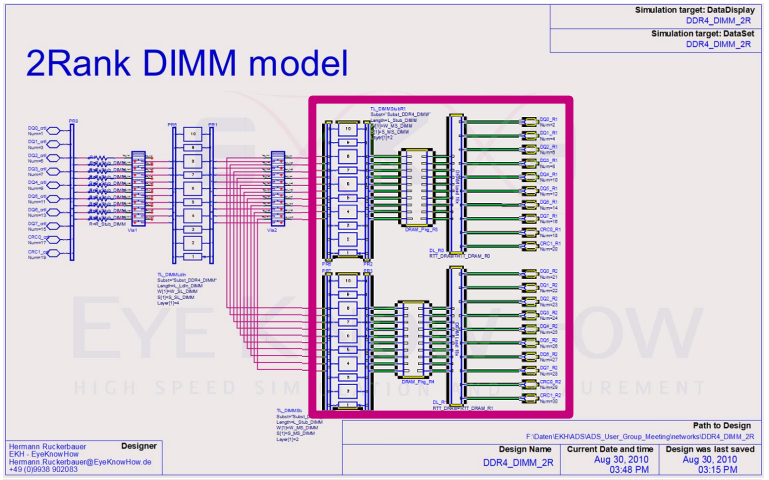
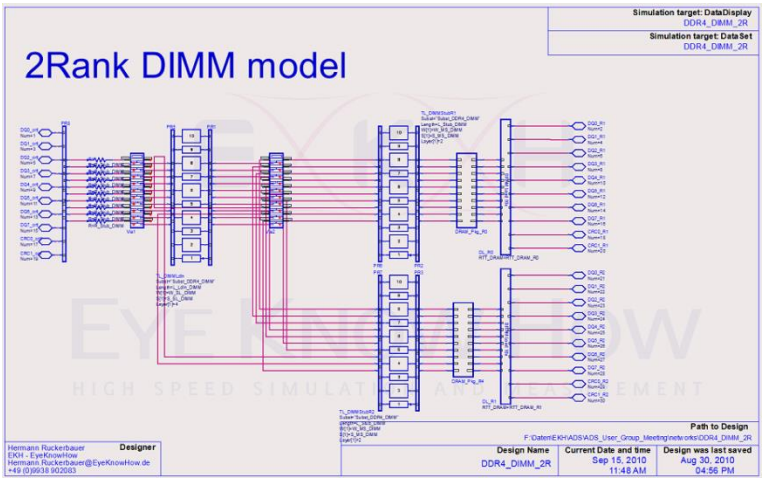
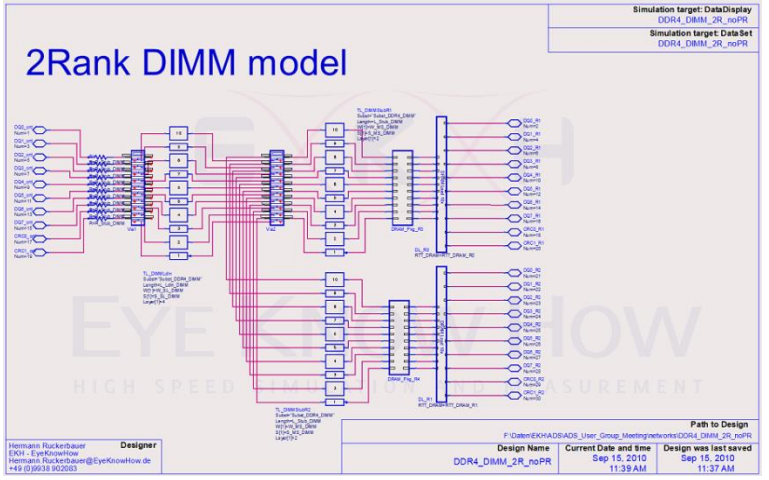
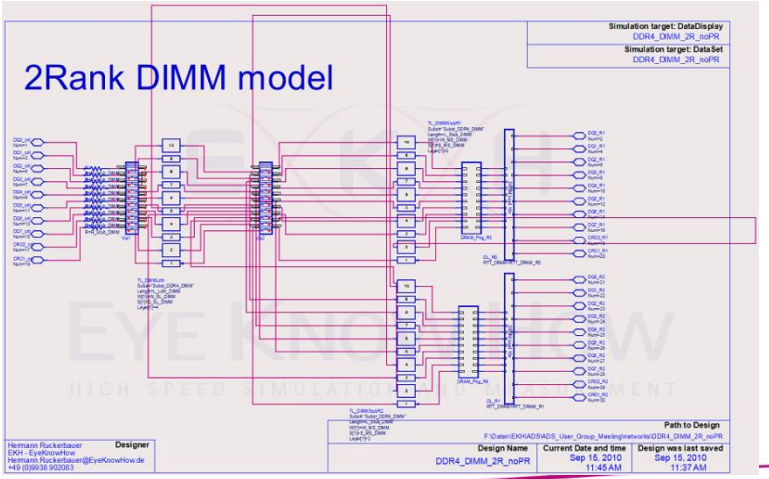
- Advantage: Simplifies the work for ADS automatic re-wiring when shifting components!









2) Schematic Simulation
Discipline: Arrangement of Circuit

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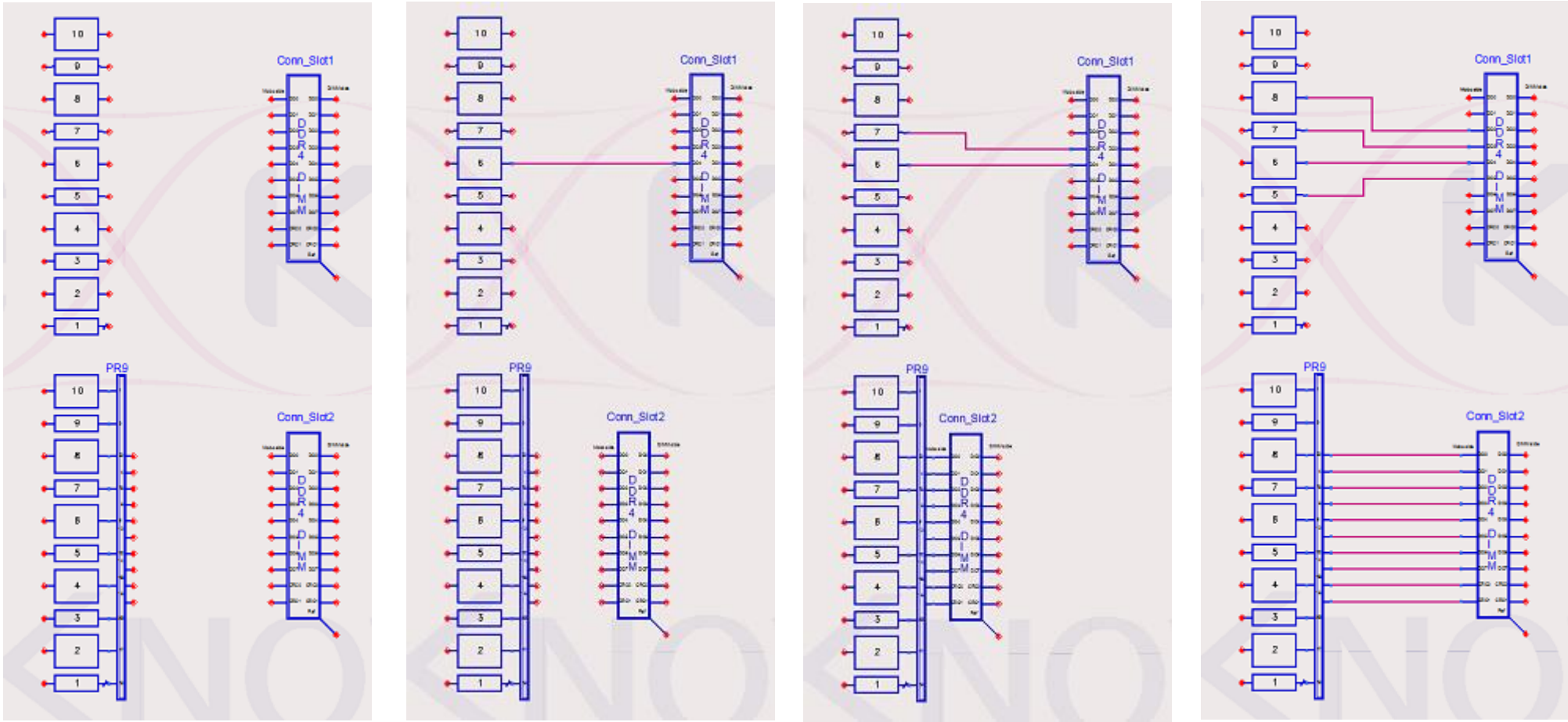
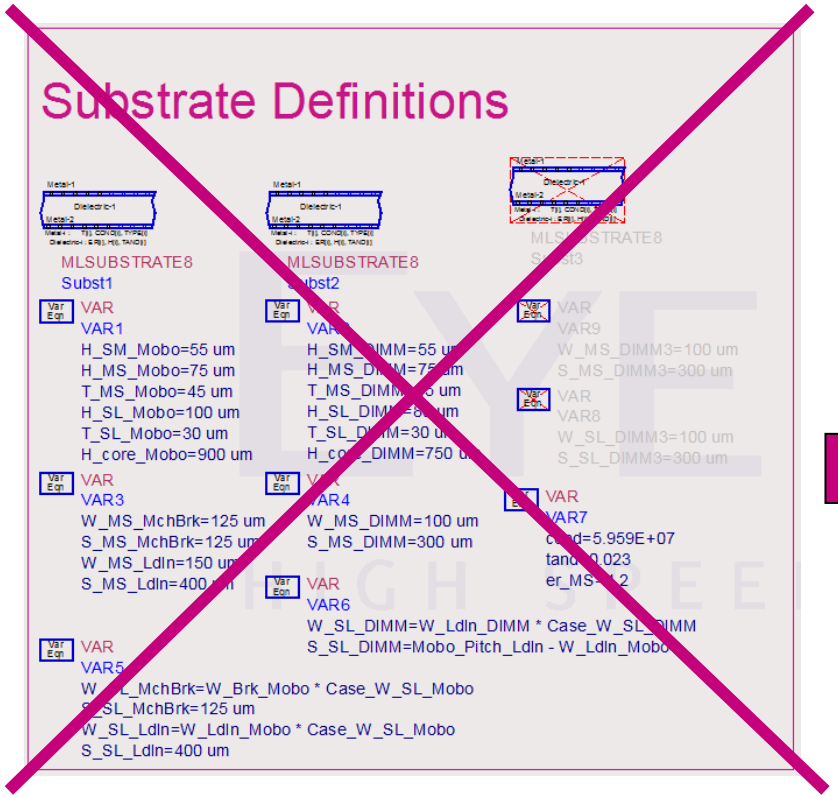
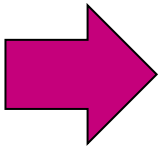
- Advantage: Connecting components faster

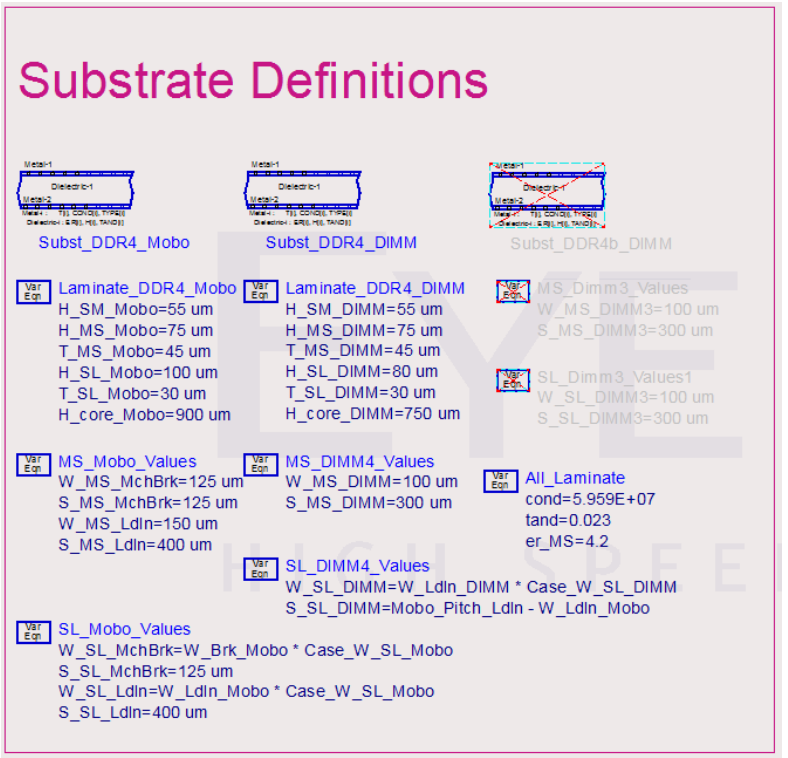


2) Schematic Simulation
Discipline: Give only important information

- Hide not required information
  - Right mouse ➔ Hide component name
- Give meaningful instance names







2) Schematic Simulation
Discipline: Simplify Documentation

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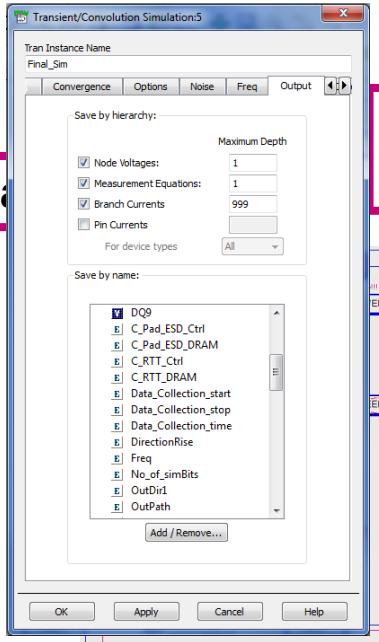
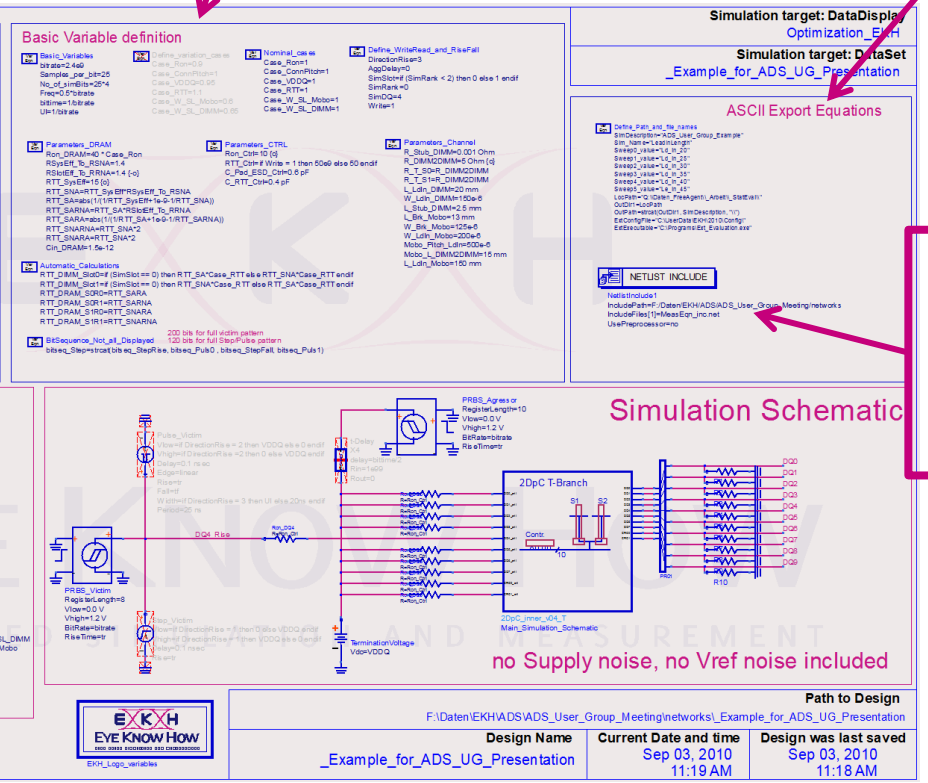
Use "Write_Var" to:
- **Export variables to ASCII file**
- **Export data/traces to ASCII file**
- **Generate batch file for automatic postprocessing with external tools**

Write all Vari

Define all simulation Parameters as Variable





Use separate Netlist:
- **Simple editing of "Write_Var" commands**
- **Create Directories by "mkdir" command**

L_Ldln_DIMM	C_Pad_ESD_Ctrl[0]
25.00 m	600.0 f

Display Variables in .dds for documentation

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3) 3D Multilayer EM for Momentum

4) Data evaluation with the Data Display

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6) FrontPanel routines

7) Conclusion

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3) 3D EM ML for Momentum
When to use this tool ?

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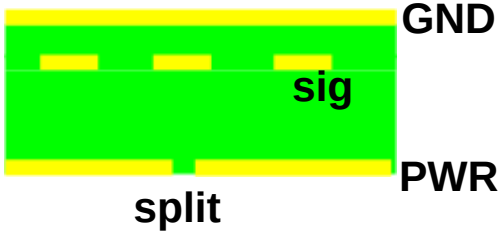
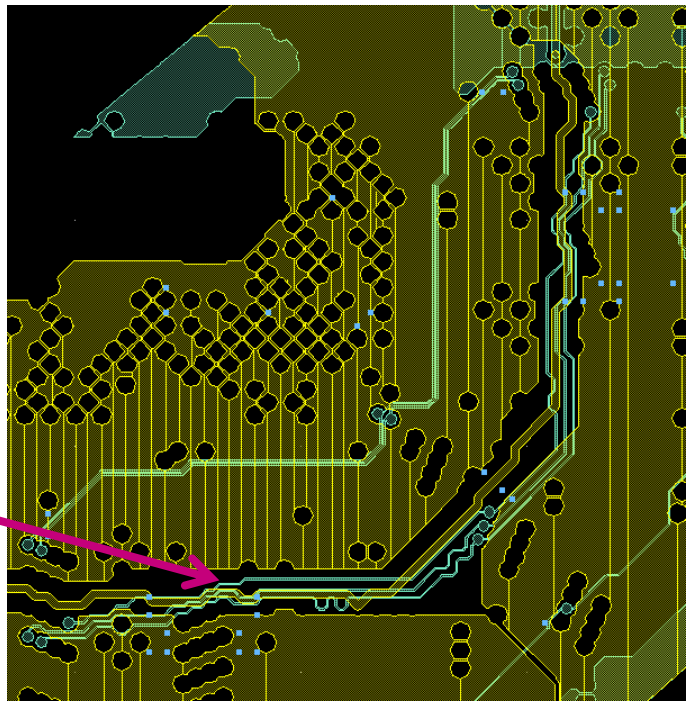
- Some structures can not be modeled with the Multilayer transmission line library
- If you need to simulate a structure with a Slot in the Reference plane the 3D Multilayer EM Field solver for Momentum is the tool of choice
- Usually such existing Layouts are too complicated to be Re-drawn. In this case it is required to transfer the Layout from the Layout tool to ADS Layout.
  - For Cadence Allegro there is a very good interface available: The Allegro DFI (Design Flow Integration)

3) 3D EM ML for Momentum
Problem Description

- In order to reduce layers an asymmetric stripline concept was chosen for an embedded board layout
  - On one side a good GND referencing was given in close proximity, while on the other side a splitted power plane in further distance was implemented.
- Target of investigation:
  - Do a check if the non ideal power referencing is causing any Problems!

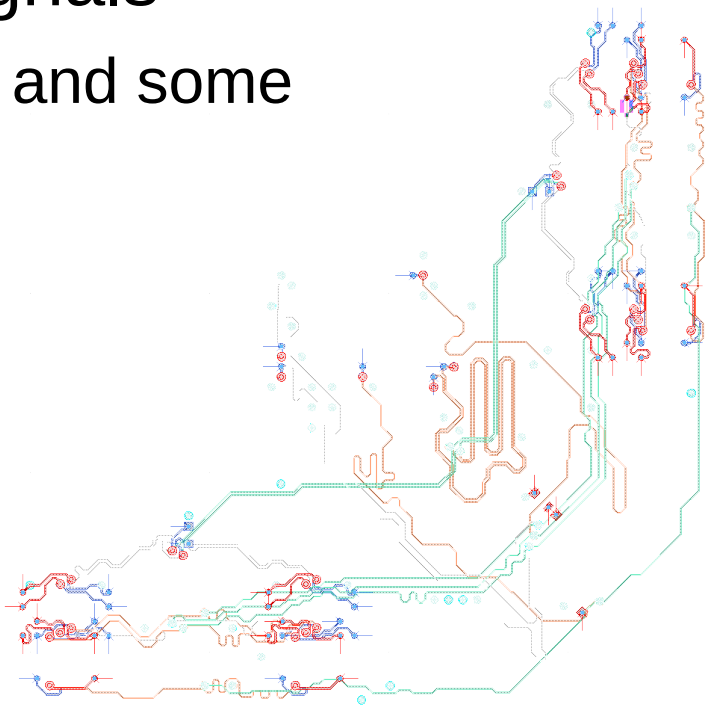


Routing over a split in the second Reference



3) 3D EM ML for Momentum
Problem Description

- This is an example where we extracted the S-Parameter for a CA bus on an embedded computer module.
- The board area was about 3x3 inches
- Signals included: 2x CLK, 4x CA signals
  - Connecting to 8 DRAMs, one controller and some Terminations this results in 62 ports!



3) 3D EM ML for Momentum
Prerequisites for the Allegro DFI

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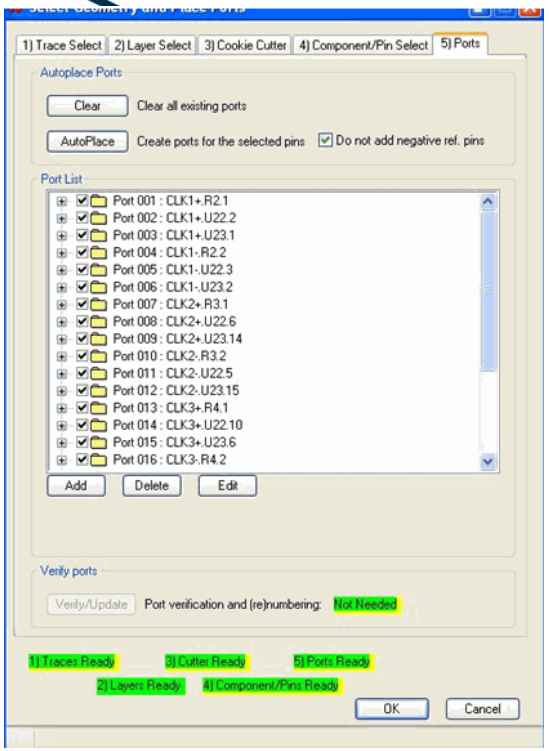

- The DFI consists of two parts:
  - The Interface in Allegro
  - The Allegro import Design kit in Momentum
- Preparation
  - Install the DFI in Allegro according to the help
  - Install the Allegro import Design Kit in ADS
  - Think about your requirements!
    - If you need a big layout you need to focus on model size reduction and reduce your accuracy settings
    - If you need an accurate high speed model you need to take a mall part of the layout with high accuracy settings

3) 3D EM ML for Momentum
The Allegro DFI interface

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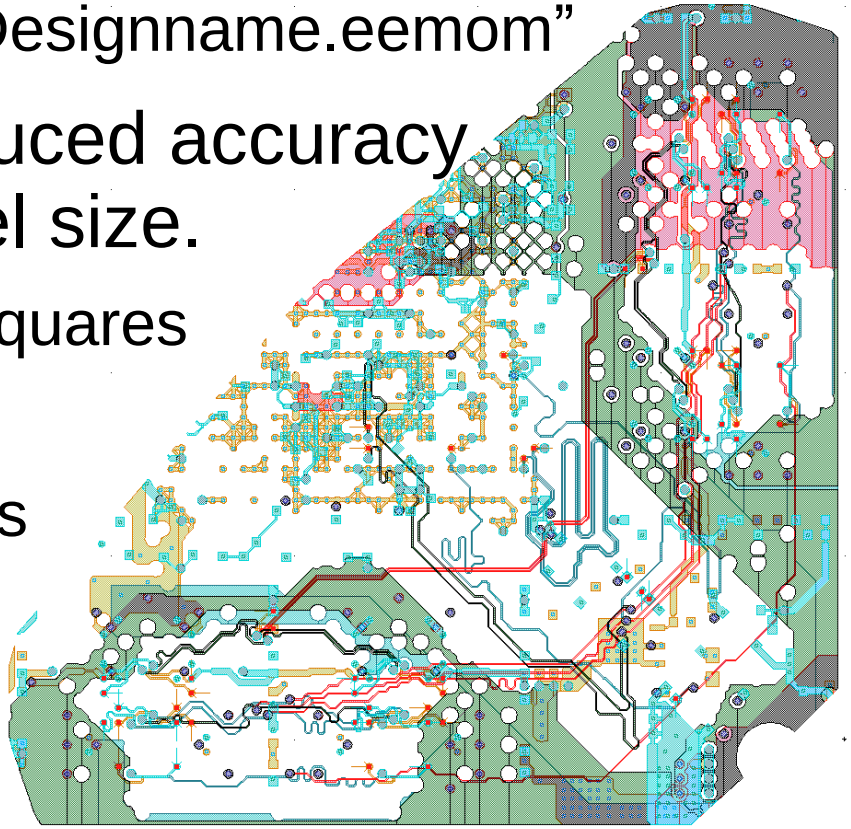
- The accuracy settings for Allegro DFI are defined in the eemom.option file
  - If a design specific file is used it needs to be in the same directory as the design and called “Designname.eemom”
- For the described problem a reduced accuracy was required to reduce the model size.
  - Vias and pads can be exported as squares
  - ARC resolution can be reduced
  - GND holes could be skipped, but this was done during the simplification in ADS



Imported Layout
Only signal layers

3) 3D EM ML for Momentum
Simplification in Momentum

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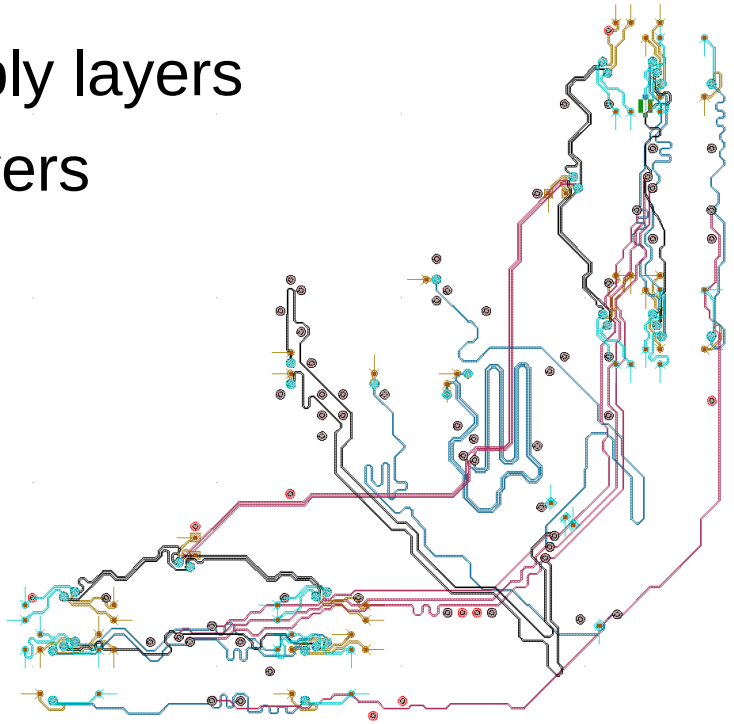
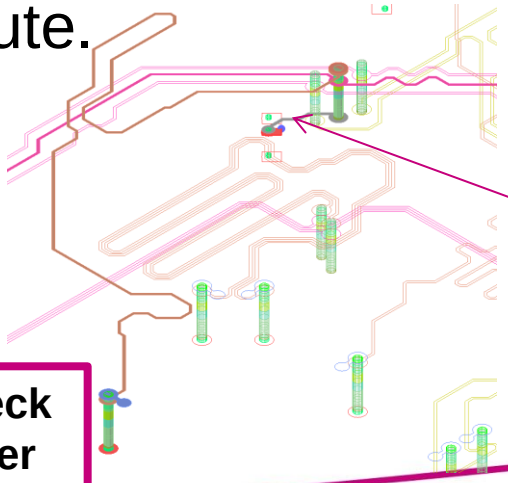
- To get a reasonable model size the layout needs some further simplification in Momentum
  - Convert Strip to Slot supply layers
  - Remove not required vias
  - Remove not required openings in Supply layers
  - Delete not required metal on Signal layers



Simplified Layout
Only signal layers

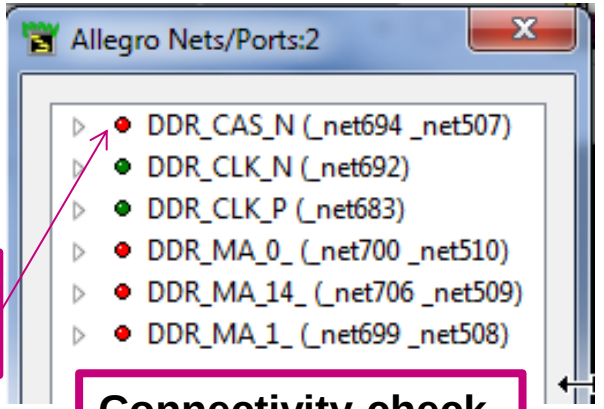
3) 3D EM ML for Momentum
Connectivity check in Momentum

- During Simplification it is possible to delete something that is still needed ➔ **Often check the connectivity!**
  - Several connectivity checks are implemented in Momentum
  - A fast and easy check is available under "Allegro Tools ➔ Allegro Nets!
    - This can have problems with routing on slot layers
  - The connectivity check in the 3D viewer works for this as well, but takes longer to execute.



Connectivity check with the 3D viewer

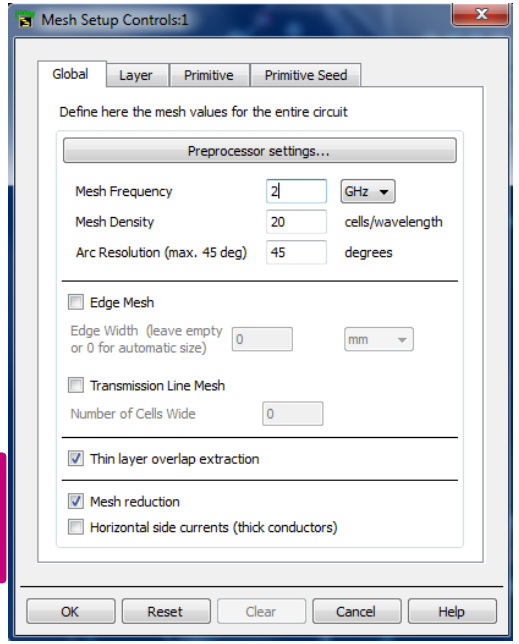
CAS Slot Routing



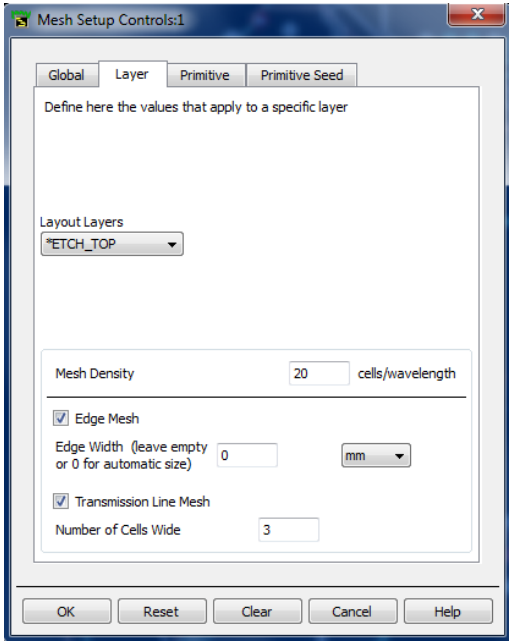
Connectivity check with "Allegro Nets"

3) 3D EM ML for Momentum
Preprocessing and Settings in Momentum

- Further methods to reduce simulation time
  - Preprocessing with “Layout Healing”, “Shape Merging” and “Layout simplification” enabled
  - Meshing and Simulation settings
    - Enable Edge Mesh only for signal layers using layer based settings



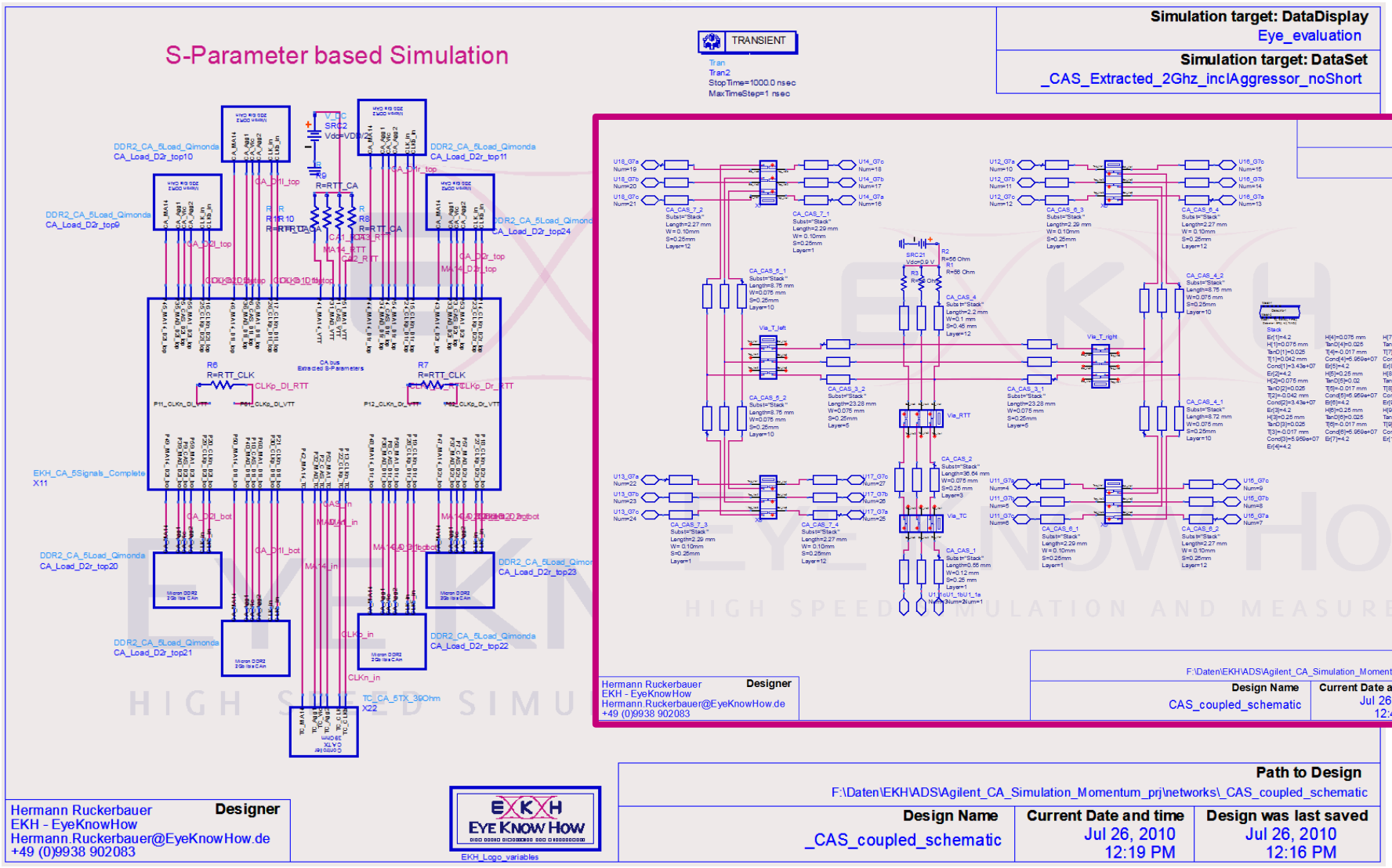
Global Mesh settings



Layer based Mesh settings

3) 3D EM ML for Momentum

Final Transient simulation



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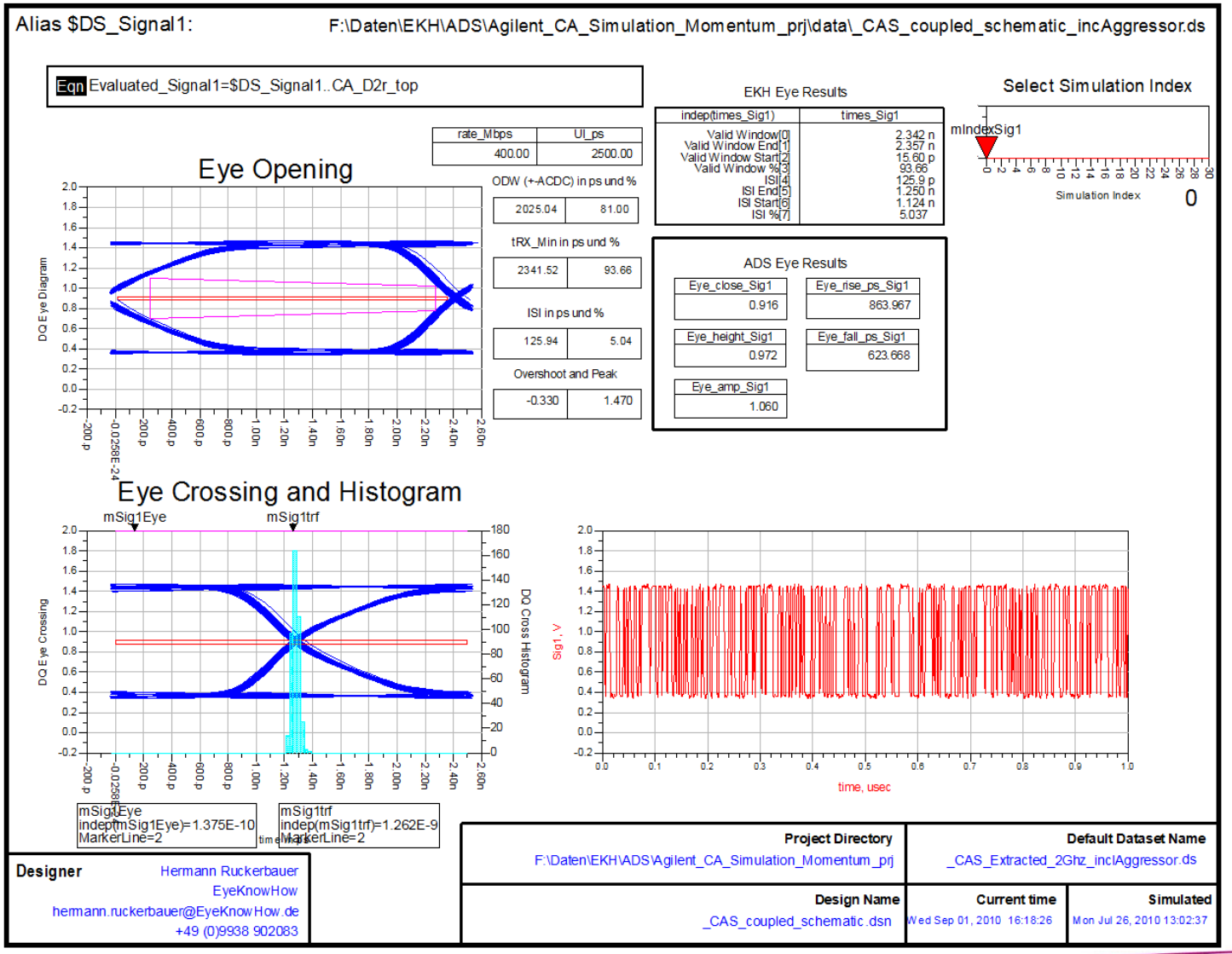
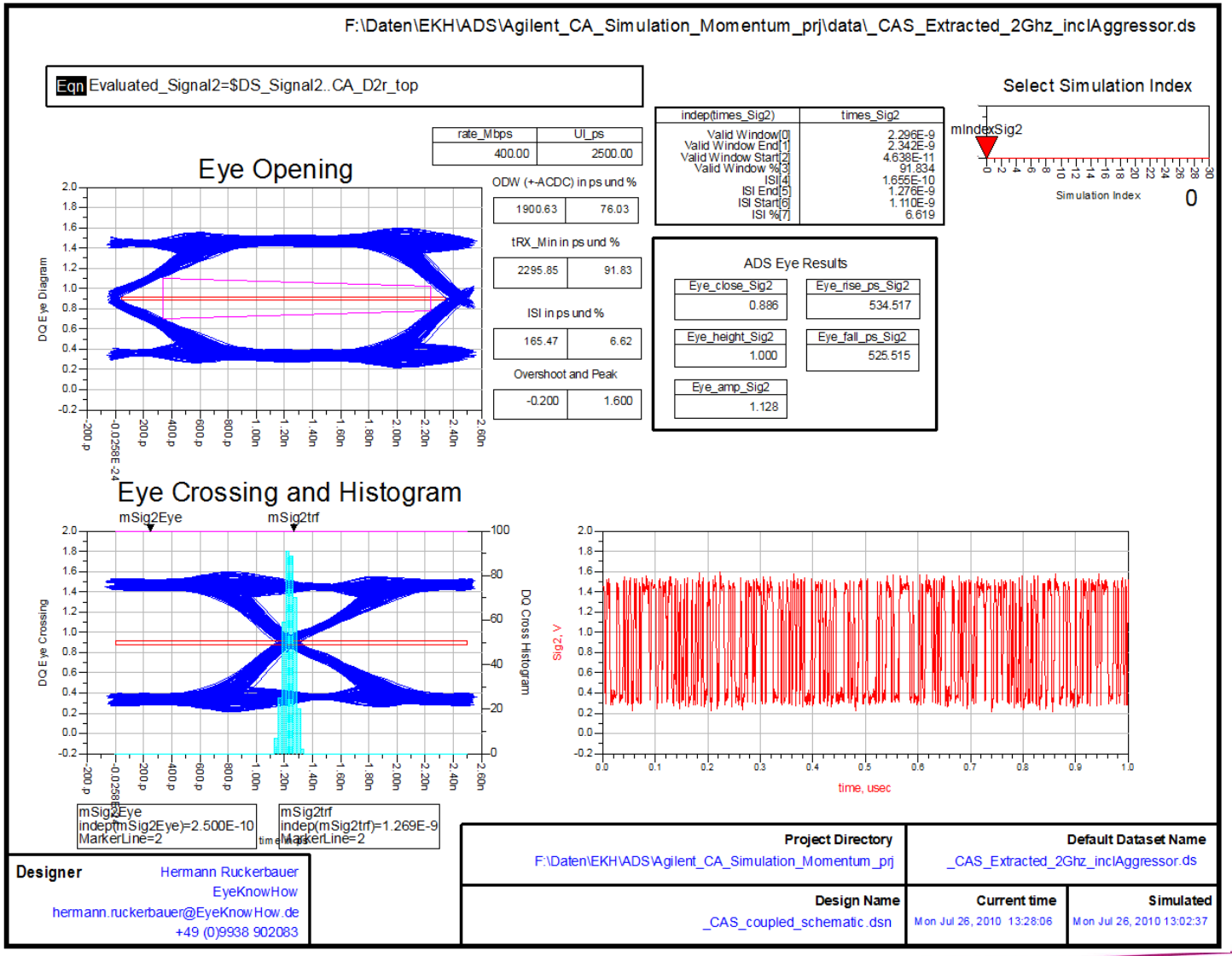
4) Data Evaluation

Simulation Results: Multilayer T-Lines

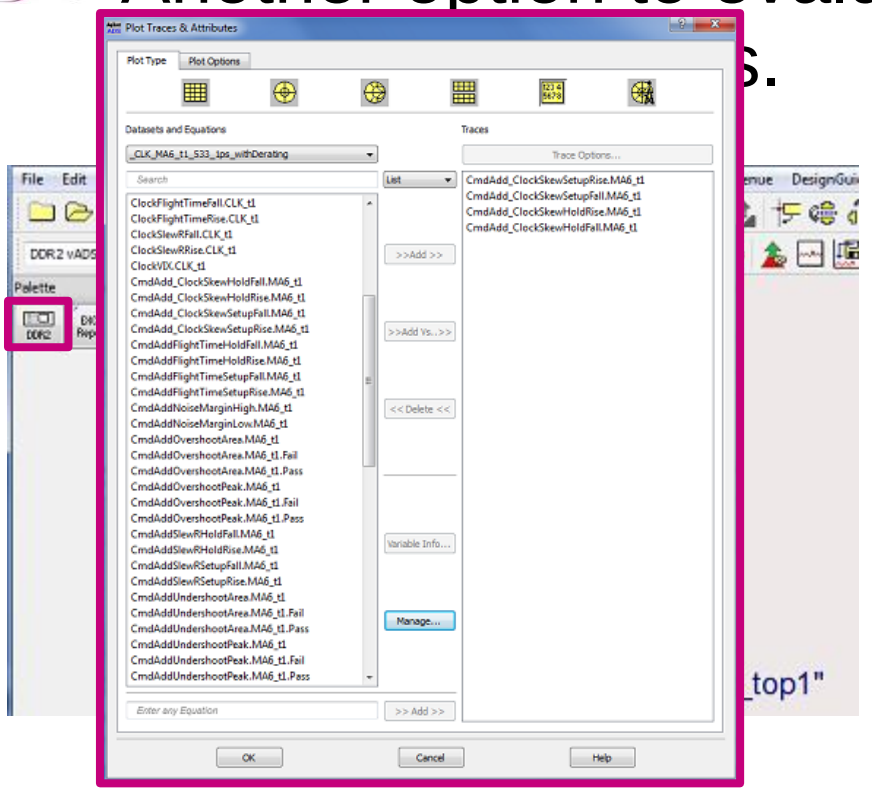


4) Data Evaluation
Simulation Results: S-Parameter



4) Data Evaluation DDR2/DDR3 Design Kit

- Another option to evaluate DDR2/DDR3 simulations are
  s.

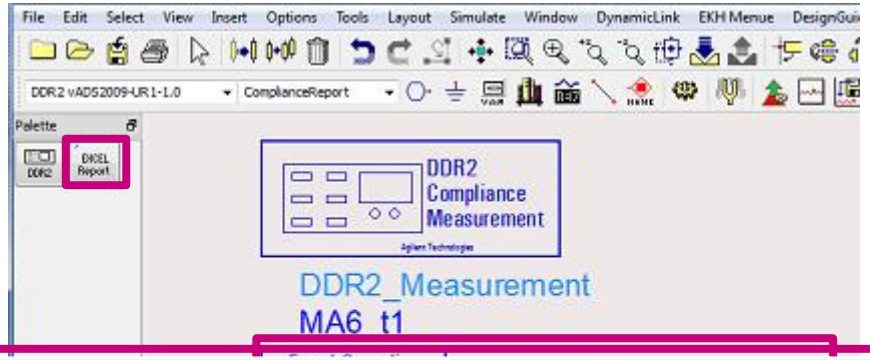


Index	...etupRise.MA6_t1	...SetupFall.MA6_t1	...HoldRise.MA6_t1	...HoldFall.MA6_t1
1.000	322.505	310.636	-55.132	-49.349
2.000	321.481	311.025	-56.010	-50.362
3.000	322.991	364.654	-110.759	-74.597
4.000	530.344	363.308	-73.709	-72.568
5.000	398.833	362.338	-117.505	-72.284
6.000	533.291	424.338	-116.248	-106.536
7.000	532.599	422.272	-75.610	-102.234

4) Data Evaluation
DDR2/DDR3 Design Kit

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

- With the Excel Report a nice report file is written

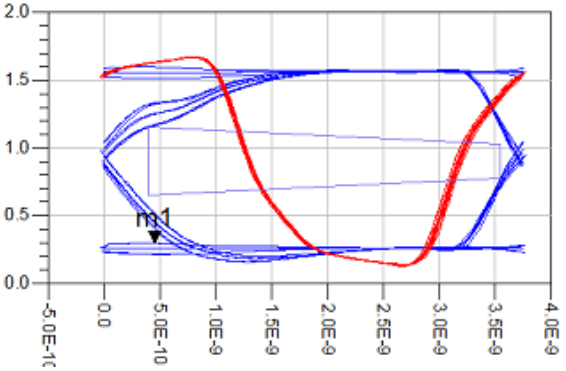


urement	Signal	Minimum	Maximum	Average
dd_ClockSkewSetupFall	MA6_t1	310,6360812	424,3375578	365,5100146
dd_ClockSkewSetupRise	MA6_t1	321,4806629	533,2914575	423,1491912
dd_ClockSkewHoldFall	MA6_t1	-106,5358198	-49,34885743	-75,41849373
dd_ClockSkewHoldRise	MA6_t1	-117,5047894	-55,1315254	-86,42465638

4) Data Evaluation
DDR2 Design Kit: Eye Opening

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

- EKH Eye calculations:
  - Valid Window: 3.15ns (includes Clock skew)
  - Setup+Hold = 3.09ns (no clock skew)



- DDR2 Design Kit calculation
  - Eye opening from AC crossing to DC crossing:
    UI – (max skewSetup – min skew hold)
    3750p – (533.3ps – (-117.5p)) = 3099.2ps

EKH Calculation

indep(caltst1)	caltst1
Setup time[0]	2.743 n
Hold time [1]	347.6 p
Diff Clock skew [2]	58.68 p
Valid window [3]	3.149 n
CLK skew start[4]	1.836 n
CLK skew end[5]	1.895 n
Valid window end[6]	2.243 n
Valid window start[7]	-906.4 p
Delay[8]	3.082 n
vref[9]	900.0 m

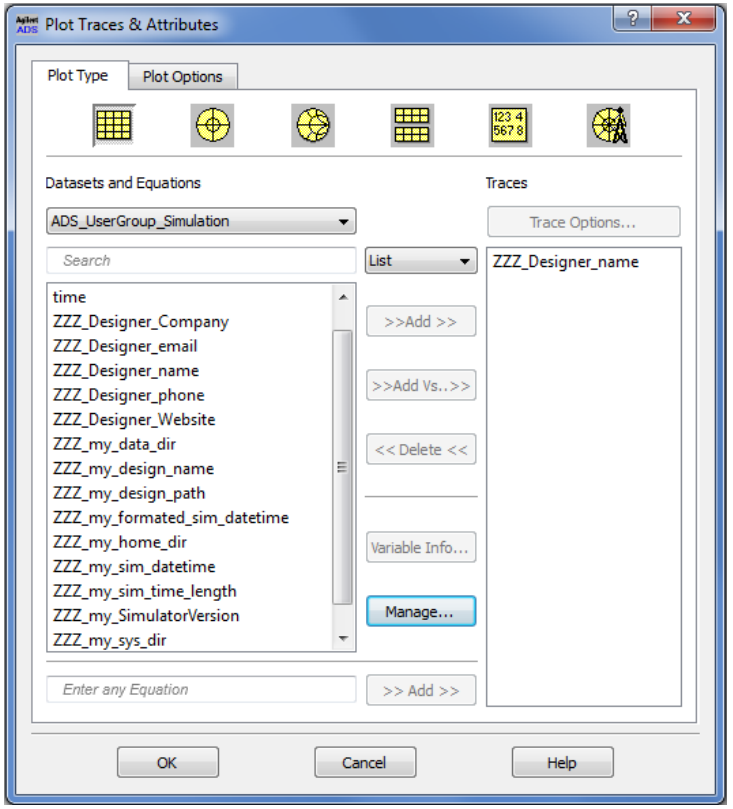
- Difference:
  - Design kit is cycle based (and more accurate)
  - EKH calculation is Eye based (and a bit overcritical)

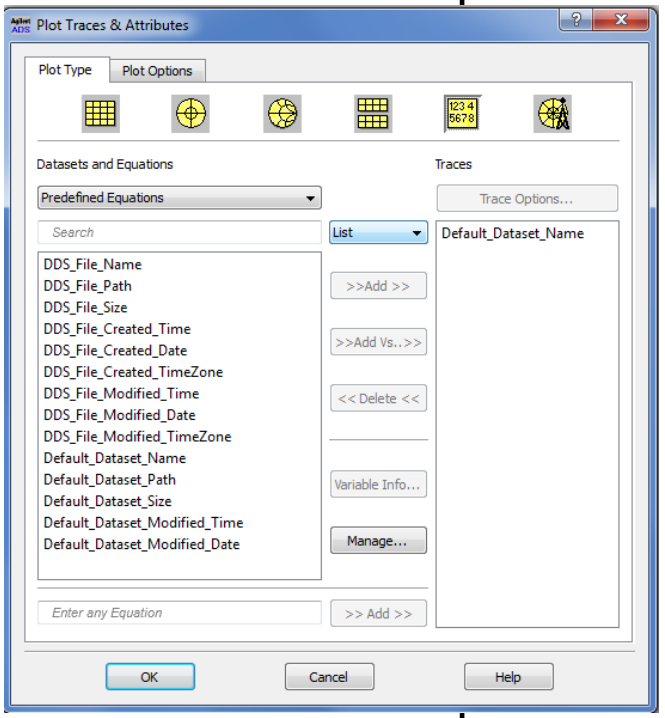
Measurement	Signal	Minimum	Maximum	Average
CmdAdd_ClockSkewSetupFall	MA6_t1	310,6360812	424,3375578	365,5100146
CmdAdd_ClockSkewSetupRise	MA6_t1	321,4806629	533,2914575	423,1491912
CmdAdd_ClockSkewHoldFall	MA6_t1	-106,5358198	-49,34885743	-75,41849373
CmdAdd_ClockSkewHoldRise	MA6_t1	-117,5047894	-55,1315254	-86,42465638

DDR2 Design Kit results

4) Data Evaluation
Using Templates and Predefined Equations

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT





Variables from Design

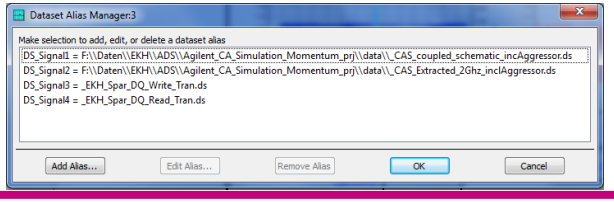
Predefined Equations:
Default_Dataset_Name

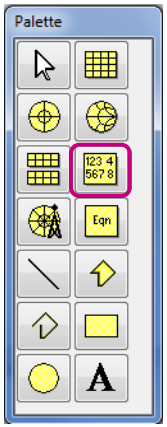
Designer Hermann Ruckerbauer EyeKnowHow Hermann.Ruckerbauer@EyeKnowHow.de www.EyeKnowHow.com +49 (0)9938 902083	**Project Directory** F:/Daten/EKH/ADS/ADS_User_Group_Meeting	**Default Dataset Name** ADS_UserGroup_Simulation.ds
	Design Name ADS_UserGroup_Simulation.dsn	**Current time** Wed Sep 01, 2010 12:40:54
		Simulated Wed Sep 01, 2010 12:42:06

4) Data Evaluation
Used Data Display Features

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

Use Alias to have simple access to different datasets in one data display

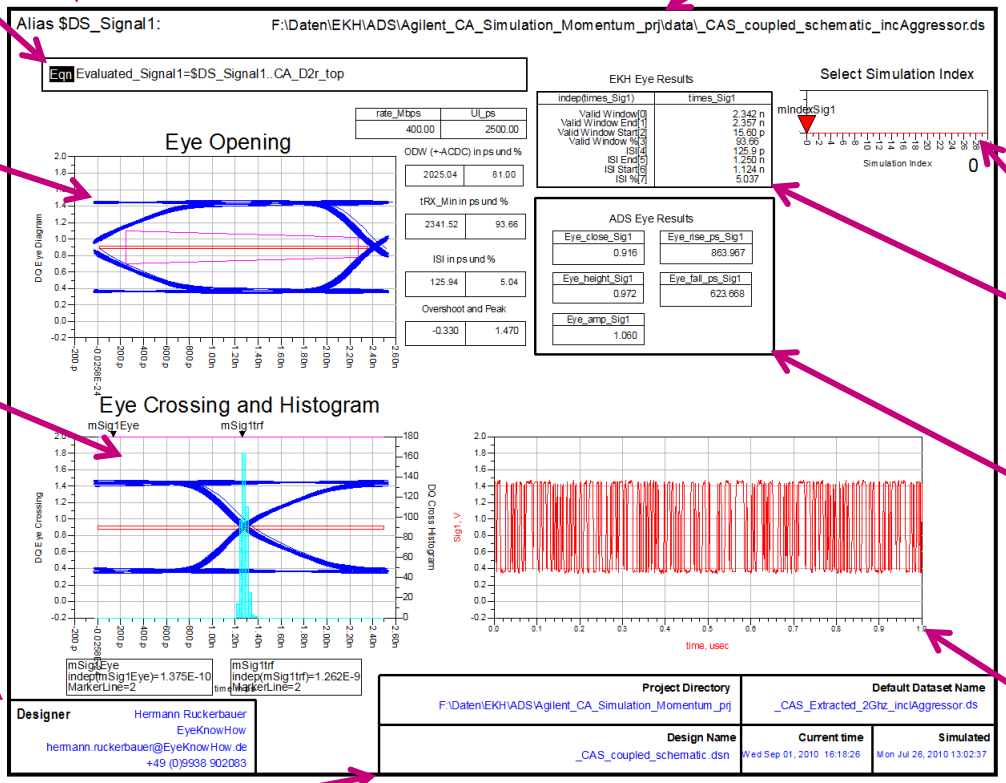




Adjust only a single variable to change content

Plot Type: List / Variable: Alias name (e. g. “DS_Signal1”)

EKH Eye Functions (incl. “DRAM Mask”)



Slider Marker for simple sweep select

EKH Eye Calcutions

ADS Eye Functions

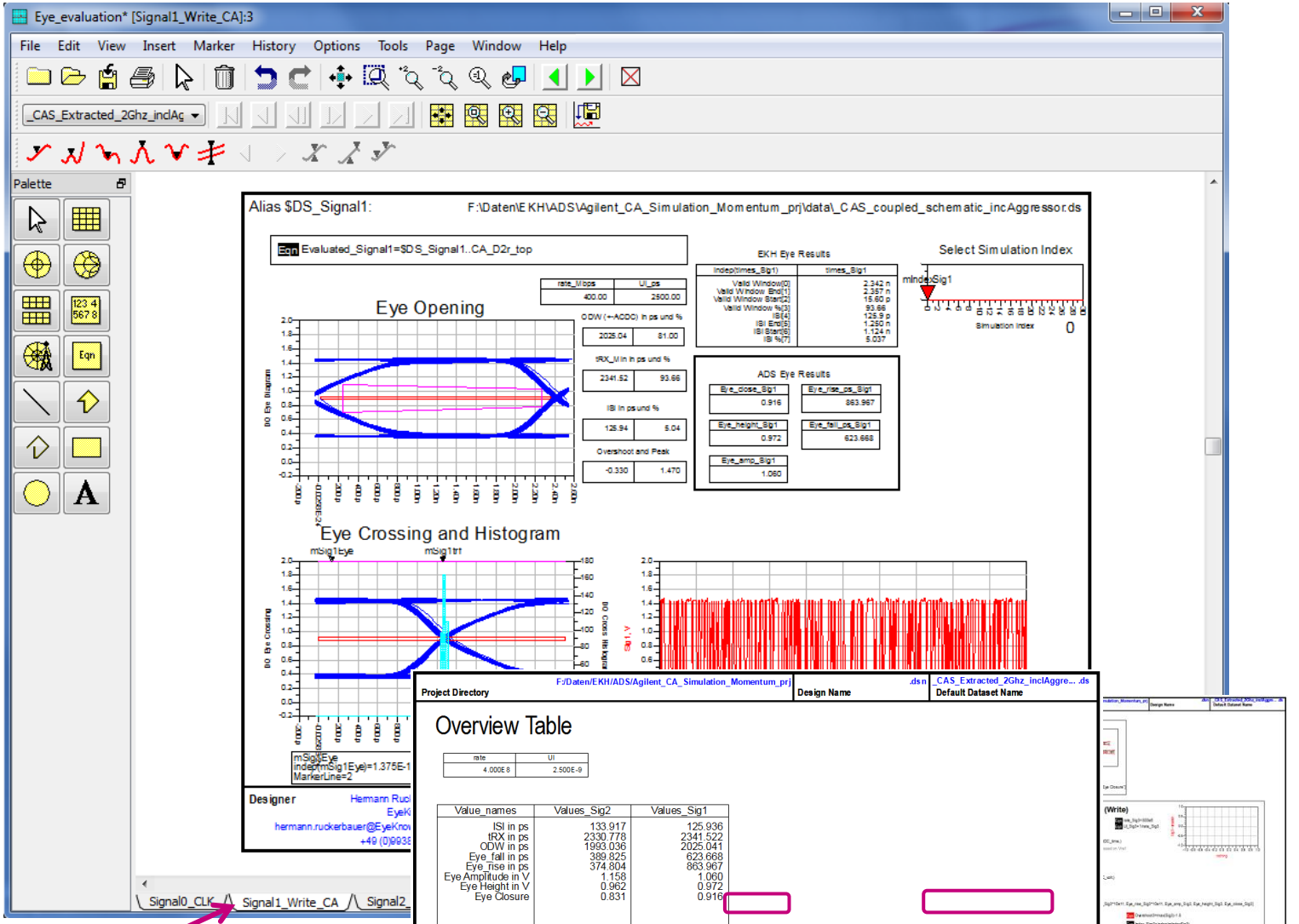
ADS Eye Calculations

Simulation variables

Just Transient Trace

Predefined Equations

4) Data Evaluation
Use Tabs



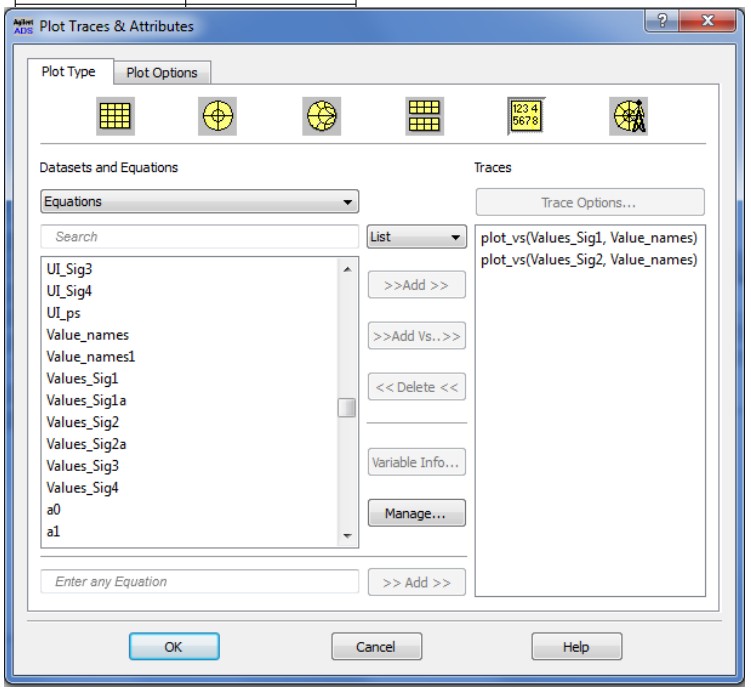
Use Tabs for hiding calculations

4) Data Evaluation
Manual Table Format

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

Project Directory	Design Name	Default Dataset Name
F:/Daten/EKH/ADS/Agilent_CA_Simulation_Momentum_prj	.dsn	_CAS_Extracted_2Ghz_inclAggre... .ds

rate	UI



Overview Table

ADS List format

ISI_ps_Sig2	ISI_ps_Sig1	tRX_ps_Sig2	tRX_ps_Sig1
133.917	125.936	2330.778	2341.522

Hermann Ruckerbauer
hermann.ruckerbauer@EyeKnowHow.de
+49 (0)9938 902083
EyeKnowHow
Designer

Fri Sep 03, 2010 14:06:55
Current time

Simulated

Agenda

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

1) Introduction

2) Analog/RF Schematic Simulations

3) 3D Multilayer EM for Momentum

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6) FrontPanel routines

7) Conclusion

8) Backup

5) 3D FEM Simulation
When to use this tool ?

- We have seen a Momentum simulation of a large PCB with reduced accuracy in order to get the simulation done.
- If the signal rates require a high accuracy then the 3D EM FEM field solver is the tool of choice
  - This gives a high level of accuracy, but
  - This can only handle small structures
- Predestinated usage for the 3D EM FEM tool:
  - Bond wires in a package
  - Vias on a PCB or in Silicon
- Following the optimization of a differential via for 10Gb data rates

5) 3D FEM Simulation
Problem Description

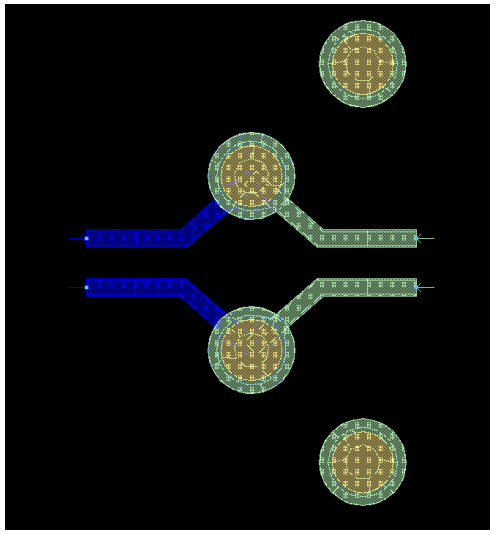
EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

- Target of the investigation was to optimize a Via based on an existing stackup for 100 Ohm differential Impedance.
- Data source was a Layout exported as ODB++ that was imported into ADS Layout.
  - Strong recommendation is to re-draw the structure and NOT to use the imported data for simulation
  - Advantages of Re-Drawing
    - Dimensions are accurate what simplifies simulation and reduces simulation time (more important than you might think …)
    - Changes are simpler as circles are Circles and not just polygons. By this it is vey easy to change e. g. the radius of a cutout

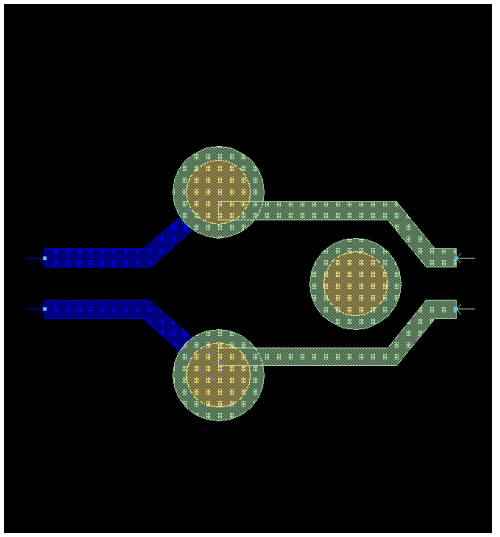
5) 3D FEM Simulation
Two Basic configurations

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

- Double Stich GND



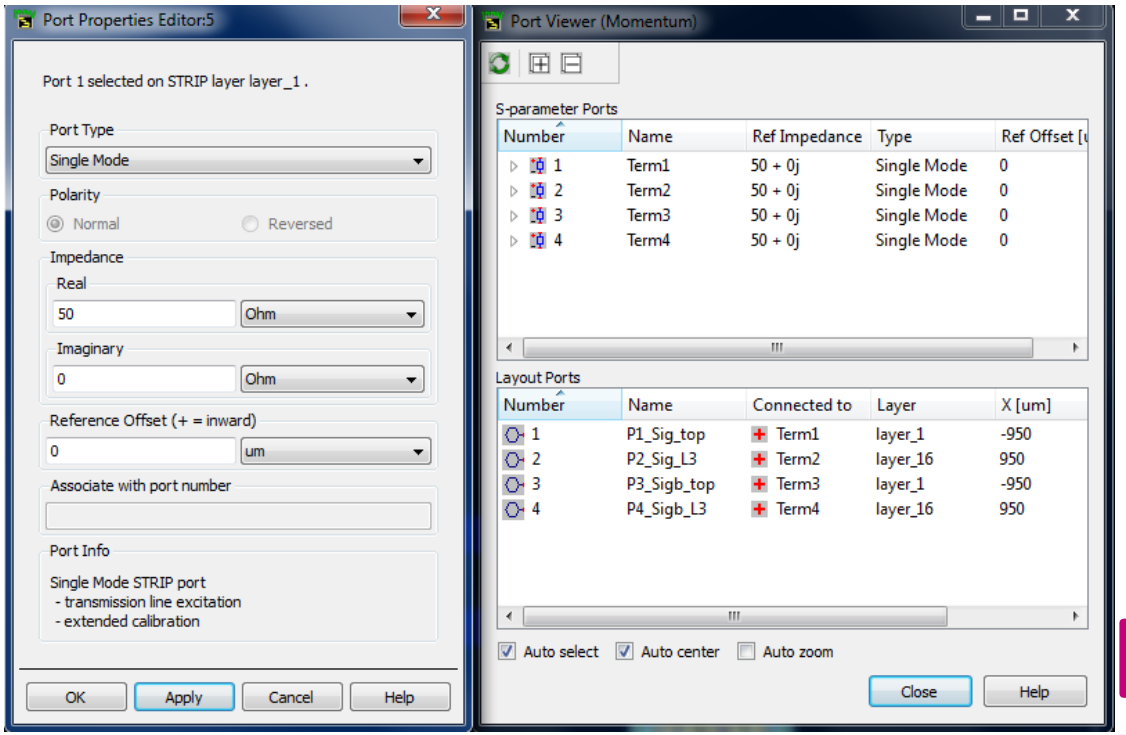
- Single Stich GND



- Parameters for Optimization
  - Number of stitch vias
  - Distance of stitch vias
  - Size of plane cutouts
  - Via pads and antipads

5) 3D FEM Simulation
Tasks for Preparation: Port Definition

- As in the 2.5D simulation: One of the most difficult things is the correct definition of the ports in the setup
  - In the Momentum example “internal” ports have been used
  - In this example “single” ports are used



Port Editor

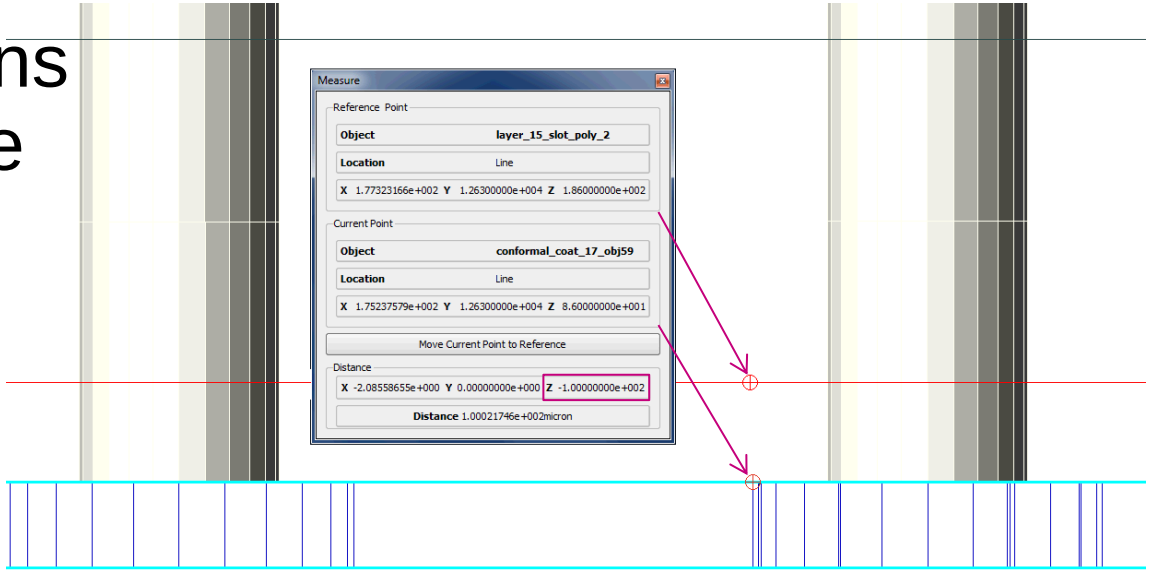
Port Viewer

5) 3D FEM Simulation

Tasks for Preparation: Substrate definition

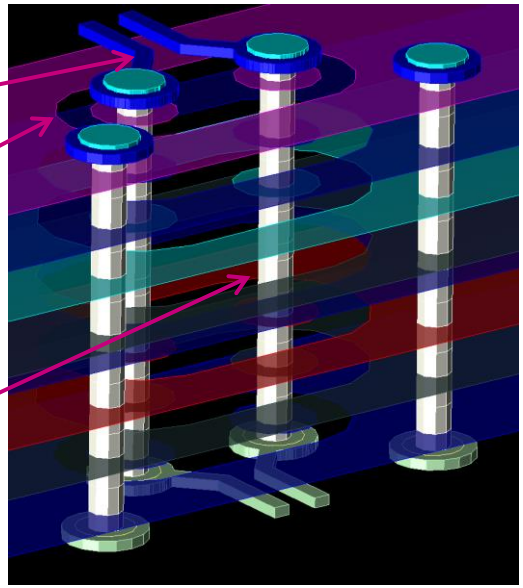
EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

- Momentum and FEM Substrate are very similar (and using the same basis)
  - Slight difference is the support of dielectric vias (e. g. for solderstop openings)
  - The definition of the Multilayer Transmissionline substrate definition is different to Momentum
- Always verify dimensions in the 3D viewer with the measurement tool!



5) 3D FEM Simulation
Final Via Definition

- In a first step the optimization was done with Momentum and the “3D Distributed” via model in the stackup!
  - This is a reasonable approach for a fast optimization
  - The final model was generated using the 3D FEM solver!
- After optimizing the dimensions we found still some possible improvements:
  - Shortly before the via the differential routing gets wider and the impedance increases
    - To compensate this the cutout on top and bottom was reduced
  - But overall the via is capacitive
    - To improve this we removed the Pads on the center Supply layers



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HIGH SPEED SIMULATION AND MEASUREMENT

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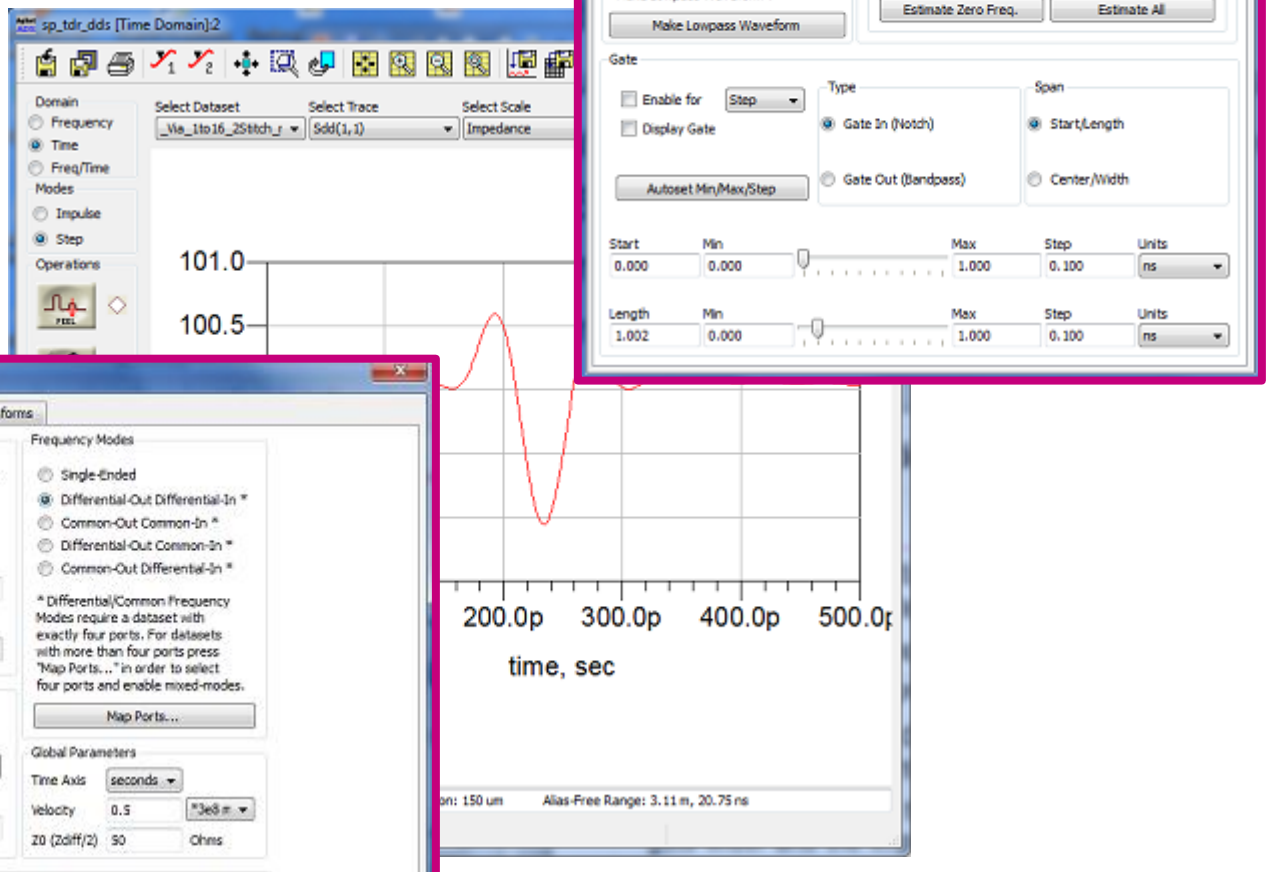
6) FrontPanel routines
Via Evaluation: SP-TDR

- The via parasitics have been evaluated with the FrontPanel SP-TDR
  - This routine calculates a TDR based on S-Parameters
- Settings used for Data evaluation
  - Define structure as Differential (“Frequency Modes”)
  - Do the evaluation from 0 to 500ps (“Transform Sweep (Time)”)
  - Velocity to 0.5 * 3e8 m/s (“Global Parameters”)
  - Delay of 1.5cm (“Port Extension”)
  - “Slight” Hamming window with a = 0.9 (“Window”)

6) FrontPane
Via Evaluation: S

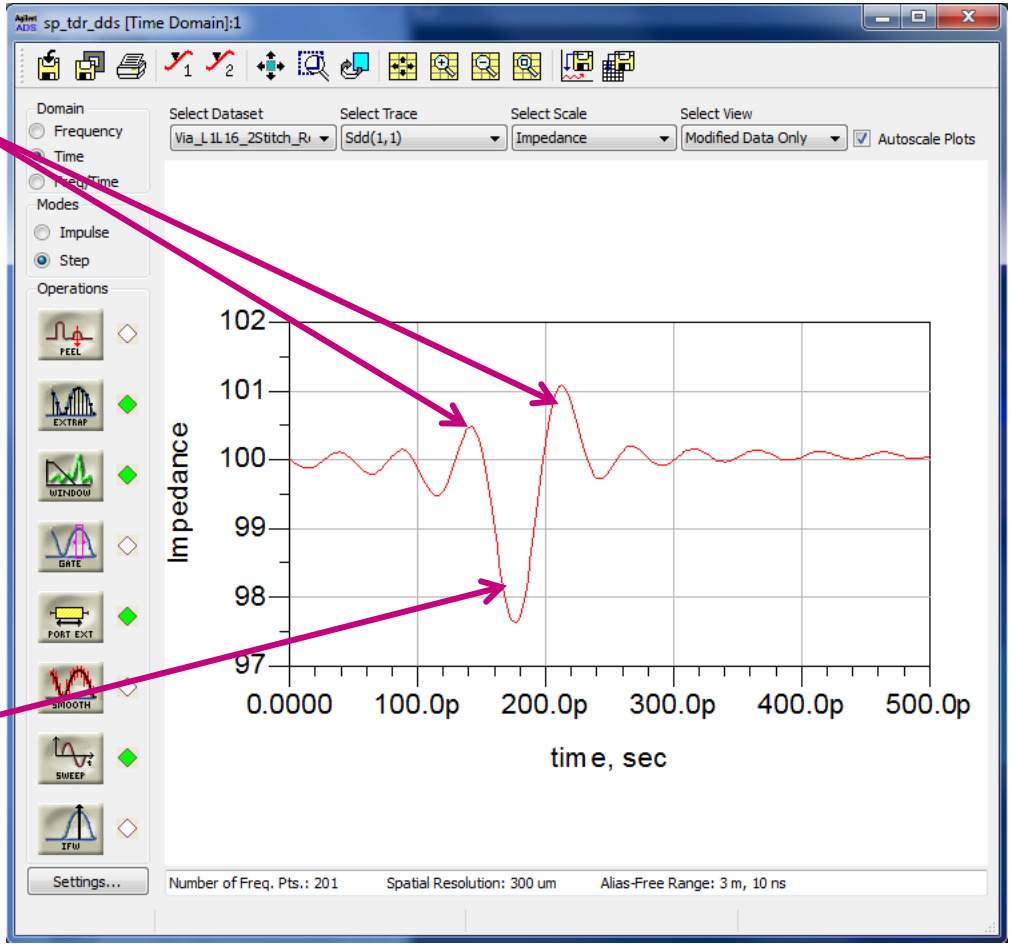


6) FrontPanel routines
Via Evaluation: SP-TDR

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

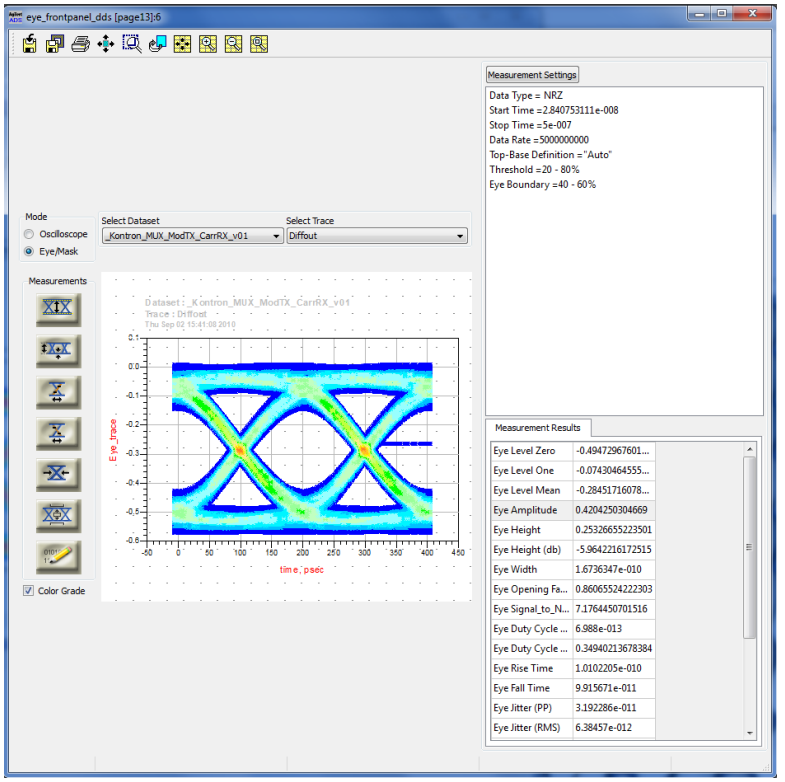
Reduction of this peaks was possible by adding C due to smaller cutout on top and bottom

Reduction of this peak was possible by reducing C due via pad removal at center supply pads!



6) FrontPanel routines
FP-Eye

- The FP-Eye routine in the Data Display is a good way to get a fast display of a dataeye without knowing any equations
  - Disadvantage is the handling:
    - Scaling of the Window
    - Difficult documentation
    - Only single eye is displayed
    - Fixed number format



- Normally we use the FP-Eye with the “Save as normal .dds” as basis for own evaluation sheets!

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7) Conclusion

- This was just a small overview how to use ADS for SI
  - There are many other parts of ADS that have not been touched
    - The digital Ptolemy system simulator
    - Model support (e. g. IBIS)
    - … and a lot more
  - Additionally a lot of interfaces to other tools and models are available
    - Matlab, HSPICE, ..
    - IBIS-AMI, X-Parameter, …
    - Hardware …
    - … and a lot more

ADS is the Swiss army knife of EDA!

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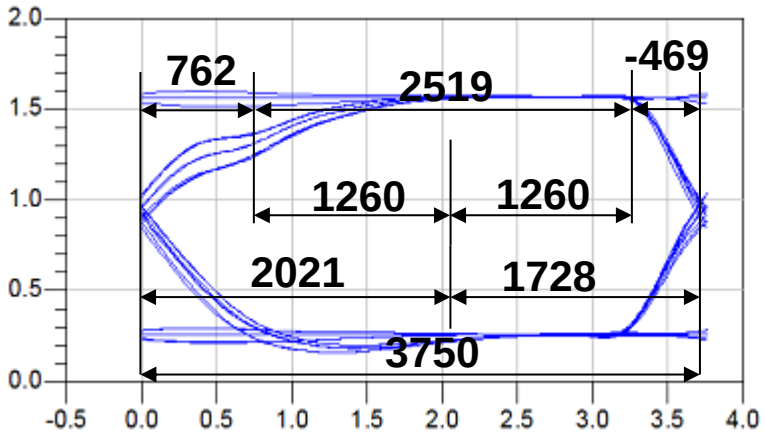
4) Data Evaluation
DDR2 Design Kit: Clock delay

- To simulate the correct Crosstalk the clock needs to be delayed by around 0.5 tck.
- But this does is not the perfect adjustment to get symmetric setup and hold margins.
- It is difficult, but possible to calculate the perfect clock delay out of the measurements from the DDR2 Design kit
- This clock delay can be used to calculate setup /hold times for the DRAM

4) Data Evaluation
DDR2 Design Kit: Clock delay

Setup/Hold @ 533
tSetup = 250p
tHold= 375p

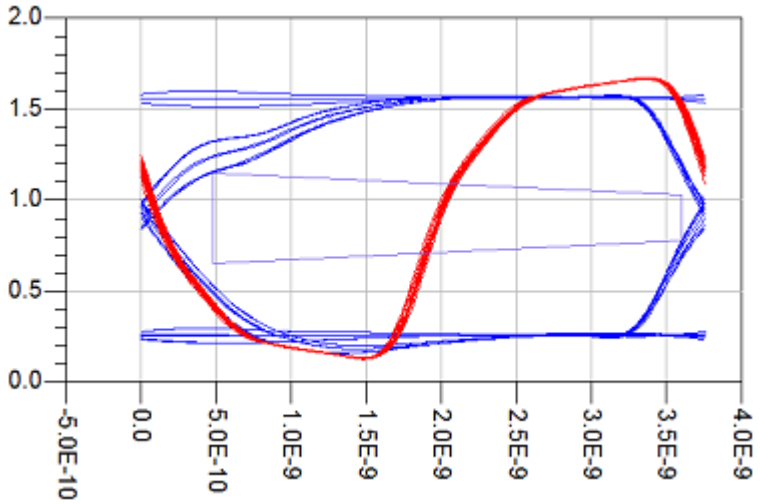
- Add DRAM tSH to skew:
  - Max SetupSkew + tsetup = 512ps + 250 ps = 762ps
  - Min Holdskew - thold = -94ps – 375ps = -469 ps
- A delay of 2.02ns would place the clock perfectly
  - Need to add the flight time difference between CLK and CA!
  - This was calculated based on Slew Rate, Flight Time Clock and Flight time CA to 185ps
  - Or can be simulated …
  - A 2.2ns delay was added to the CLK



Probe	Measurement	Signal	Minimum	Maximum	Average
MA6_t1	CmdAdd_ClockSkewSetupFall	MA6_t1	395,1531007	449,6923219	425,9007699
MA6_t1	CmdAdd_ClockSkewSetupRise	MA6_t1	396,6127588	512,82657	448,8582792
MA6_t1	CmdAdd_ClockSkewHoldFall	MA6_t1	-79,7608975	-3,208134984	-45,58591197
MA6_t1	CmdAdd_ClockSkewHoldRise	MA6_t1	-94,28593739	-8,268098824	-56,13336704

4) Data Evaluation
DDR2 Design Kit: Clock delay

- EKH Eye Calculation (tSH not considered in Measurement)
  - Setup Margin: 1.469 – 0.250 = 1.219
  - Hold Margin: 1.581 – 0.375 = 1.206



indep(caltst1)	caltst1
Setup time[0]	1.469 n
Hold time [1]	1.598 n
Diff Clock skew [2]	58.75 p
Valid window [3]	3.126 n
CLK skew start[4]	1.813 n
CLK skew end[5]	1.872 n
Valid window end[6]	3.470 n
Valid window start[7]	343.9 p
Delay[8]	1.851 n
vref[9]	900.0 m

- For a final Timing Budget calculation there is only missing the information on Controller output timings