Eye Know How

Signal Integrity Consulting

Services and KnowHow
Company Facts

Founder: Dipl. Ing. (FH) Hermann Ruckerbauer

Founded: March 2009

Location: Itzlinger Strasse 21a, 94469 Deggendorf (Bavaria), Germany

Network partners in:
- Munich (Design, Layout, CAD)
- Straubing (EMV)
- Deggendorf (Lab)
- China (Shandong und Shaanxi): Oulong Consulting
Hermann Ruckerbauer
Background

- Study of Micro System Technology at University of Applied Sciences in Regensburg
  - Dipl. Ing. (FH) Micro System Technology
- 15 Years experience in Memory Development and High-Speed Signaling
  - Siemens: Bench and Production test
  - Infineon / Qimonda:
    - High Speed Signaling
    - Application test
  - Interface standard definition
- Holder of many patents
- EEE Publication:
  - Cascading Techniques for a High-Speed Memory Interface
EKH Services

- Consulting for High Speed Signaling
- Consulting for Memory Implementation
- High speed Simulation and Measurement
- Power Delivery Simulation
- Model Generation
- Measurements
  - E. g. Logic Analyzer, Scope, TDR, VNA
- Failure Analysis
- PCB Design and Layout
- Layout and Design Reviews
- Pre-Compliance Measurements on Serial Links
  - E. g. USB2/3, PCIe 2/3, SATA; HDMI, …
- Compliance Measurements on Memory Busses
  - E. g. DDR2/3/4, LPDDR 2/3, GDDR3/5, …
**EKH Cooperation Partners**

- **DKH – DesignKnowHow: Dr. Abdallah Bacha**
  - PCB Design and Layout
  - RF Topics

- **SinePulse: Md Sayfullah (www.sinepulse.com)**
  - IT services (India)
  - Hardware development (e.g. FPGA)

- **FH Deggendorf (www.fh-deggendorf.de)**
  - Measurement Lab with VNA and TDR
  - PCB X-section

- **BitIfEye**
  - Measurement Lab for high speed digital signals

- **Rohde&Schwarz**
  - Automated VNA up to 67GHz
EKH Cooperation Partners

- **EMV – Testhaus** (www.emv-testhaus.de)
  - EMI / EMC compliance test

- **PCB Manufacturing**
  - Ilfa (www.ilfa.de)
  - Elekonta Marek (www.elekonta.de)

- **Assembly**
  - Mair Electronics (www.mair-elektronik.de)
  - Beflex Electronic (www.beflex.de)

- **China Business (Peter Poechmueller)**
  - Oulong Consulting (www.ouulongconsulting.com)
Happy Customers

- Bosch
- TQ – Systems
- Kontron
- Congatec
- Micron
- 3D-Plus
Software Tools

Keysight ADS (former Agilent)
- Time and Frequency domain simulation
- Analog and Digital Simulation
- 2.5D and 3D field solver
- Data evaluation (measurement and simulation)

Power Delivery
- Cadence Power SI (former Sigrity)
- Keysight ADS

Design and Layout
- Cadence Allegro
- Mentor Hyperlinx/Pads
Software Tools

- **Offline Scope Software**
  - Keysight Infiniium Offline
  - Amherst M1 OT Ultimate

- **S-Parameter post processing**
  - AtaiTec Corp. ADK, x2D, SI3D, and ISD

- **EyeKnowHow internal Software**
  - ADS Data Evaluation: AC/DC Memory Eye Opening
  - DDR Protocol Analysis
  - Cadence to ADS (Layout to Schematic) conversion
Agenda

1) Memory System and Device KnowHow
2) Signal and Power Integrity Simulation
3) Signal and Power Integrity Simulation
4) 2.5D and 3D Modeling for e.g. PCB Layout and Vias
5) Measurement based Modeling
6) Compliance and Correlation Measurement
7) Physical Failure Analysis
8) Design and Layout Services
9) System Optimization
10) EMC / EMI Measurement and Consulting
11) Software and Hardware Products
Memory System KnowHow

- Worked in the development of DDR1 / DDR2 / DDR3 / DDR4
  - Data and Command/Address bus architecture development
  - Memory Device Specification
- Consumer, Mobile, Desktop and Server system understanding
  - Differences in requirements and boundary conditions
- System requirements
  - Cache line size limitations
  - Turnaround times, Bandwidth and latency
  - Power limitations
- Clocking
  - SSC, Random and Deterministic Jitter
- Controller functionality
  - Controller PCI register features (e.g. Delay shift, Driver strength, digital timings)
Close interaction between System Architecture and DRAM features
- IO specification (e.g., Input capacitance, driver and termination linearity)
- DLL functionality
- Memory Device Specification

DRAM Core / architecture / process limitation
- Source for Latency
- ODOC package and impact on Architecture
- DRAM process and impact on speed and parasitics

DRAM packaging
- Planar and stacked DRAM parasitics
- Wirebond and FCIP packaging

Single Die DRAM Package
Signal Integrity Simulation

- **Time Domain simulation**
  - Spice models (Lumped elements and BSIM Transistor based)
  - S-Parameter
  - IBIS

- **Frequency Domain simulation**
  - S-Parameter Model Generation
  - Model Comparison

- **Statistical Data Evaluation**
  - Adding Random and Deterministic Jitter
  - Channel Characterization by Step Response

- **Data Eye evaluation**
  - Setup/Hold Evaluation
  - Timing Budget Calculation

Eye Diagram from Channel Step Response
Signal Integrity Simulation
Schematic Example

2Rank DIMM model
Signal Integrity Simulation
Schematic Example

Subcircuit Schematic

Subcircuit Symbol
Electro-Thermal simulation

Electro-Thermal simulation simulation considering thermal impact from devices and PCB copper resistance

Temperature distribution on a PCB with thermal vias including device power loss and copper resistance power loss.
Power Integrity Simulation
Impedance of Power Delivery

Simulate PDN (Power Delivery Network) Impedance over Frequency

Positive Example
First Resonance @ 340MHz
Only 0.25 Ohm

Negative Example
First Resonances @ 120 – 150 MHz
Up to 3 Ohm
Power Delivery Simulation

Electro-Thermal simulation considering thermal impact from devices and PCB copper resistance

Plane current density

IR Drop of power plane

Via current density
2.5D Modeling
PCB Layout

Cadence and Mentor to ADS Layout Transfer
Simulation in Momentum

\- Result: S-Parameter Model
\- Co-Simulation with ADS time/frequency Domain Simulation
\- Signal- and Power Supply Integrity
\- Layout accurate Simulation
\- X-talk (intera- and inter layer)
\- Reflections
\- Losses

3 Coupled lines of a CA Bus on a DIMM
3D Modeling
Vias, Packages, Connectors

- ADS 3D Fieldsolver Momentum and EMDS
  - Accurate Via Modeling
  - Substrate Routing
  - Bondwires
  - FBGA Package Balls
  - Signal Traces
  - Power Planes

BACKPLANE VIA
Via L1 to L16

16 coupled Bond Wires:
Signal and Power
Measurement based Modeling
VNA / TDR based

Characterization of existing boards
- Measurement with VNA
- TDR/TDT Characterization up to 20 GHz BW

SMD Connector Capacitance

60 Ohm Routing
50 Ohm Cable
Pad Capacitance
Material Parameter and Modeling

PCB Modeling

Required models for channel simulation:
- Trace Models
- Via Models
- Package Models
- Connector Models (see next page)

Cross section of PCB with blind and micro vias
Measurement based Modeling
Testboard Design

Definition, Design and Layout of Characterization Boards

Lumped Model Fitting

Blue: Model
Red: Measurement

Testboard

Insertion Loss

FEXT

NEXT

ADS Model fitted to Measurement
Physical Failure Analysis

3D CRT
PCB Characterization

Automated Testsystem for PCB characterization up to 67 GHz

- Fully automated to get highly reproducible results
- In cooperation with Rohde & Schwarz
Losses on different PCB materials (MS)
Pre-Compliance Tests

High Speed Interfaces require verification by Compliance tests.

- Certified labs offer accredited compliance tests and are required to e.g. use the official logos.
- If the Logo is not required the alternative is a Pre-Compliance test

Advantage of Pre-Compliance tests:

- Deliver not just Pass/Fail, but can be directly starting point of debugging
- Cheaper as official tests at certified labs
- Often closer to your location as the next certified lab

Available Testsetups:

- PCIe Gen 1 / 2 / 3
- SATA Gen 1 / 2 / 3
- USB Gen 1 / 2 / 3
- HDMI
- DVI
- Display Port
Pre-Compliance test Examples

USB3 RX

Jitter Tolerance
for USB SuperSpeed Hosts

SATA TX

PCIe TX

Test Statistics

<table>
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<tr>
<th>Test</th>
<th>Failed</th>
<th>Passed</th>
<th>Total</th>
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Margin Thresholds

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<th>Warning</th>
<th>Critical</th>
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<td>&lt; 2 %</td>
<td>&lt; 0 %</td>
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### Pass # Failed # Trials Test Name, Actual Value, Margin, Pass Limits

- **0 1 System Board Tx, Unit Interval (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 109.9948 ps
  - Margin: 45.0 %
  - Pass Limits: 199.0480 ps <= VALUE <= 200.0600 ps

- **0 1 System Board Tx, Template Tests (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 0.000 ps
  - Margin: 50.0 %
  - Pass Limits: 500 nV <= VALUE <= 500 nV

- **0 1 System Board Tx, Peak Differential Output Voltage (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 044.3 mV
  - Margin: 38.7 %
  - Pass Limits: 300.0 mV <= VALUE <= 1.2000 V

- **0 1 System Board Tx, Eye-Width w/ 4th crosstalk (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 149.00 ps
  - Margin: 50.0 %
  - Pass Limits: 95.00 ps

- **0 1 System Board Tx, RMS Random Jitter w/ 4th crosstalk (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 2.793 ps
  - Margin: 94.2 %
  - Pass Limits: 48.000 ps

- **0 1 System Board Tx, Maximum Deterministic Jitter w/ 4th crosstalk (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 11.697 ps
  - Margin: 79.5 %
  - Pass Limits: 57.000 ps

- **0 1 System Board Tx, Total Jitter at BER-12 w/ 4th crosstalk (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 50.060 ps
  - Margin: 51.4 %
  - Pass Limits: 165,000 ps

- **0 1 System Board Tx, Eye-Width w/ 4th crosstalk (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 149.00 ps
  - Margin: 38.0 %
  - Pass Limits: 168.00 ps

- **0 1 System Board Tx, RMS Random Jitter w/o 4th crosstalk (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 2.793 ps
  - Margin: 94.2 %
  - Pass Limits: 48.000 ps

- **0 1 System Board Tx, Maximum Deterministic Jitter w/o 4th crosstalk (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 11.697 ps
  - Margin: 73.4 %
  - Pass Limits: 44.000 ps

- **0 1 System Board Tx, Total Jitter at BER-12 w/o 4th crosstalk (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 50.096 ps
  - Margin: 44.6 %
  - Pass Limits: 92.000 ps

- **0 1 Reference Clock, High frequency > 1.5MHz RMS Jitter (Common Clock) (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 2.212 ps
  - Margin: 28.7 %
  - Pass Limits: 3.10 ps

- **0 1 Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clock) (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 260 fs
  - Margin: 91.3 %
  - Pass Limits: 3.00 ps

- **0 1 Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clock) (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 2.54 fs
  - Margin: 36.5 %
  - Pass Limits: 4.00 ps

- **0 1 Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clock) (PCIe 2.0, 5.0 Gt/s)**
  - Actual Value: 340 fs
  - Margin: 95.5 %
  - Pass Limits: 7.50 ps
DFT Layout:
Test point placement

Dataeye @ 5.3Gb Measured vs. Simulated / Ball vs. Pad

Driver (e. g. Controller)  Measurement Point  Receiver (e. g. DRAM)

Simulated @ pad  Measurement @ via  Simulated @ via

[Circuit diagrams and waveforms showing measurement and simulation results]
# Logic Analyzer

**Digital Timing evaluation**

- Spec compliant timings / Finding timing violations
- Digital Timing Settings / MRS setting

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**Digital Timing Settings / MRS setting**

- MRS setting for specific timing analysis
- Compliance checking for digital signals

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**Spec compliant timings / Finding timing violations**

- Analysis of digital timing to ensure compliance
- Identification of timing violations

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**Eye Know How**

High speed simulation and measurement solutions from Eye Know How.
Logic Analyzer
Statistical Command sequence evaluation

Statistical Access evaluation
Performance/Power Optimization

Timings:
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Name  Min  Max
RAS_bank_0 12 2025
RAS_bank_1 259 2025
RAS_bank_2 450 2020
RAS_bank_3 1874 2030
RAS_bank_4 - -
RAS_bank_5 - -
RAS_bank_6 - -
RAS_bank_7 573 573
RAS_rank 12 2030

Name  Min  Max
RC_bank_0 16 2150
RC_bank_1 761 2158
RC_bank_2 718 2182
RC_bank_3 2032 2122
RC_bank_4 - -
RC_bank_5 - -
RC_bank_6 - -
RC_bank_7 - -
RC_rank 16 2182

Name  Min  Max
RP_bank_0 4 124
RP_bank_1 5 1763
RP_bank_2 5 268
RP_bank_3 5 142
RP_bank_4 - -
RP_bank_5 - -
RP_bank_6 - -
RP_bank_7 1089 1089
RP_rank 4 1763

Timings:
- AL=3
- BL=4
- RL=4
- TCCD=2
- TFAW=14
- TPDN=0
- TRAS=12
- TRC=16
- TRCD=4
- TRFC=54

Name  Min  Max
RFC 55 55
REFI 2072 2091
RRD 3 2070
CCD 2 77
Failure Analysis
Software Memory test: Decoding

Memory test failure Analysis
- Evaluate log files from Software Memory tests
- Narrow down failure reason
- DQ vs. CA related fail
- Single DQ vs. DQS fail
- Read vs. Write fail
- Device vs. Signal integrity related fail
- Vref Margin test implementation
- Adjust VREF until fail and evaluate fail behavior
- Timing Margin test implementation
- Change Controller delays (DQS and CLK) until fail and evaluate fail behavior

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<td>FAILURE: possible bad address line at offset 0x00000000 = address 0x099C0038</td>
<td>FAILURE: possible bad address line at offset 0x018A5141 = address 0x062D4504</td>
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<td>Re-Read:</td>
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<tr>
<td>Expected value F663FFC7, Read value 099C0038</td>
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</tbody>
</table>

Skipping to next test...
Design and Layout
Xilinx FPGA based Test board

DRAM Characterization Testboard
Simulate and measure Backplane e.g. 10G Base – KR

- Fitted Attenuation (FA)
- Insertion Loss (IL)
- Insertion Loss Deviation (ILD)
- Insertion Loss to X-talk (ICR)
Physical optimization for High speed Signaling

Stackup Design
- HDI proven and high speed Stackup
- High speed material

Routing Design

Via Design
- Optimize via to 100 Ohm
- Optimize connector pin field: Via + BreakOut Routing

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Advanced Glass Reinforcement Technology for Improved Signal Integrity

Presented at the HyperTransport™ Technology Developers Conference October 2007

By Russell Dudek, Compunetics, Inc.
Patricia Goldman & John Kuhn, Dielectric Solutions, LLC
Interference Radiation Test

System Specification Limits (e.g. for PC, Server)
Data Evaluation
EKH ael DRAM Eye routines

ODW: Multi Signal open Data Window

Multiple Eyes incl. Timing Reference

tSetup line

tHold line

ISI line
Examples with some Details: EKH Eye visualization

- **AC/DC based eye aperture**
  - DQ Eye Diagram
  - Time: 0.0 ns to 1.200 ns

- **Flight time based timing calculation**

- **Eye Overlay**

- **ISI at Vref**
  - DQ Eye Diagram
  - Time: 0.0 ns to 1.200 ns

- **Slew Rates**
ComExpress Carrier Board Characterization

- Unique Testboard for direct connection to high speed traces on ComExpress Carrier board
- Simulated and optimized up to 20GHz
- Improved Material
- All high speed lanes connected to SMA
- De-embedding of Test Fixture possible
Memory Interposer for DRAM Compliance Testing

Available as Service or Product
For DDR2/3/4, x4/x8/16, Planar or Stacked

High Performance, Low Parasitic’s
- Can be de-embedded
- Wing Design for flexible usage with maximum DRAM size and minimum Board spacing
- High accurate embedded resistors