New Features in (LP)DDR5

A short overview

Details are explained in EKH's seminar
"Open the Black Box of Memory"

https://ee-training.dk/training/open-the-black-box-of-memory-f2f

DRAM specification: evolution of DRAM standards

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Comparison of system key features:

Key feature	SDR	DDR1	DDR2	DDR3	DDR4	DDR5
Per pin data rate [Mb/s]	66 – 133	200 – 400	400 – 1066	800 – 2133	1600 – 3200	2000 - 8400
Channel (64/32bit) bandwidth [GB/s]	0.53 - 1.06	1.6 – 3.2 (64bit bus)	3.2 – 8.5 (64bit bus)	6.4 – 17.0 (64bit bus)	12.8 – 25.6 (64bit bus)	12.8 – 25.6 **(32bit bus)**
Slots per channel	4 ... 8	4 (6 ... 8)	3 (4)	2 (3)	2	2
Termination for Cmd/Addr/Clk bus	None	Motherboard	Motherboard Hybrid T CA bus	DIMM to VTT FlyBy CA bus	DIMM to VTT FlyBy CA bus	**On die** to VDDQ CA bus
Termination for data bus	None	Motherboard and memory controller	SDRAM (ODT) and memory controller to VTT	SDRAM (Dynamic ODT) and memory controller to VTT	SDRAM (Dynamic ODT) and memory controller to **VDDQ**	SDRAM (Dynamic ODT) and memory controller to **VDDQ**
Synchronization for Cmd, Addr, Clk bus	SE clock	Differential clock	Differential clock	Differential clock	Differential clock	Differential clock
Synchronization for data bus	SE clock	Single ended strobe	SE and Diff. strobe	Differential strobe	Differential strobe	Differential strobe

LPDDR4 vs. LPDDR5: SDRAM device overview

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Comparison of device key features:

	LPDDR4 SDRAM	LPDDR5(X) SDRAM
Mb/s per pin	20 - 4266	10 - 3200 (CKR = 2:1) – 8533 (CKR = 4:1)
I/O organization	Dual channel x16 per die ➔ x32 (and others)	Single channel x16 die, x32 package (and others)
VDD (1) [V]	1.8 (1.7 – 1.95)	1.8 (1.7 – 1.95)
VDDQ (IO Buffer) [V]	1.1 (1.06 – 1.17) / 0.6 for LPDDR4(X)	Range-1: 0.5 (0.47 – 0.57) (ODT enable) Range-2: 0.3 (0.27 – 0.37) (ODT disable)
VDD2 (Input Buffer) [V]	1.1 (1.06 – 1.17)	Dual VDD2 rail: VDD2H = 1.05 (1.01 – 1.12) & VDD2L = 0.9 (0.87 – 0.97) Single VDD2 rail: 1.05 (1.01 – 1.12)
Max. Density [Gb]	Up to 16Gb per Channel per die	Up to 32Gb per Channel per die
Number of Banks	2x8b	BG, 8b, 16b
Prefetch	2x16n	16n, 32n
Burst length	16, 32 (on the fly)	16 (BG and 16B mode), 32 (8B) mode
Strobe	Differential	Differential, single-ended for low frequencies
DQ driver strength	RZQ / 1,2,3,4,5,6 ZQ calibration	RZQ / 1,2,3,4,5,6 ZQ calibration
Termination	Command based for DQ ODT pin controlled for CA (LPDDR4 noX)	Different termination values for CA and DQ ODT can be chosen in MR11. No ODT pin!
Strobe signaling	Differential DQS	Differential RDQS and WCLK
DQ signaling	Single-ended **VSSQ** terminated	Single ended **VSSQ** terminated
CLK signaling	Differential	Differential, single-ended for low frequencies
CA signaling	Single-ended SDR **VSS** terminated Multi-cycle commands	Single-ended, DDR, **VSS** terminated, lower CLK speed, Multi-cycle commands
Interface spec	LVSTL	LVSTL

DDR3/4/5 Memory
ODT functionality

- DDR3:
  - DQ ODT only, controlled by ODT signal routed to NonTarget Ranks for enabling ODT without Command and Commands (dynamic ODT)
  - CA passive SMD terminated on DIMM/Board at the end of FlyBy bus (no ODT)
- DDR4:
  - improved DQ ODT with e. g. support of Per Rank Power down
  - same CA passive board termination as DDR3
- DDR5:
  - Fully command controlled DQ ODT with NonTarget Commands
  - CA ODT with two groups, for configurable FlyBy bus termination
    - Different CA termination configuration (resistance value per DRAM) for CLK/CS/CA possible

LPDDR Memory
ODT functionality

- LPDDR4:
  - DQ bus: MR and command controlled ODT
  - In LPDDR4X also CA bus is completely MR and command controlled and ODT(CA) pin is ignored
    - LPDDR4 still used a static ODT signal for configuration
- LPDDR5:
  - DQ bus: MR and command controlled ODT including NT (Non Target) commands
  - CA bus: MR and command controlled ODT
    - different configuration for CLK/CS/CA possible

DDR/LPDDR Memory
Termination voltages / schemes

- DDR4:
  - DQ bus: High level termination to VDDQ
  - CA bus: passive SMD R Termination on board to VTT=VDDQ/2 (equivalent to Thevenin termination)
- DDR5
  - High level termination to VDDQ for all Signals
- LPDDR4/5
  - Termination to GND for all Signals

DDR/LPDDR Memory
Command Address bus protocol

- DDR4:
  - Conventional SDR CA bus with 18 Addresses, 3 Bank Addresses, 2 Bank Group Addresses, reuse of A14-A16 as RAS/CAS/WE and additional Act_n Command
  - 1 Command per clock cycle
- DDR5
  - 14 signal SDR CA bus, up to 2 clock cycles long multicycle commands
  - No dedicated function assigned any more to a specific pin
- LPDDR4
  - 6Pin wide SDR CA bus, up to 4 clock cycles long multicycle commands
  - No dedicated function assigned any more to a specific pin
- LPDDR5
  - 7Pin wide DDR CA bus, up to 2 clock cycles long multicycle commands
  - No dedicated function assigned any more to a specific pin

DDR/LPDDR Memory
Refresh functionality

- LPDDR5 introduces tREFW and clarifies where tREFI comes from
  - Array is refreshed completely with 8192 Refresh cycles during tREFW!
- (LP)DDR5 are reducing tREFW to 32ms
  - With 8192 refreshes tREFI is reduced to 3.9us!
- (LP)DDR5 “hides” Refreshes and shortens dead time after Refreshes by splitting up refreshes (on cost of sending more Refresh commands) with features like
  - Fine Granularity Refresh (less Rows refreshed, but still blocks access to the DRAM)
  - Refresh Same Bank or Refresh per Bank (allows to access other banks, while 1 bank is refreshed
- DRAMs tell the controller about required Refresh rate by Readout of Moderegisters
  - This readout gives not an absolute number for Temperature, but just the information how many refreshes are needed for the current temperature.

LPDDR5 DQ signaling
LPDDR5 DQ Write

- New signaling with a Write Clock “WCK” introduced
  - DQ Write uses WCK: Write Clock as timing information like DQS in the past
  - Unidirectional Signal ➔ only from Controller to DRAM
  - 2:1 or 4:1 Frequency WCK:CK
    - Dependent on Speed below or above 3200Mb/s
  - Need to be synchronized before Write Data to the DRAM
    - Can be in “Always on” mode
  - Single ended support for speeds <1600Mb/s
    - SE support also for CK and RDQS
- Read data is also sent back based on WCK timing information
  - But Read DQS signal is still available and can be enabled if needed

(LP)DDR5 signaling
Input Mask for System Signal Integrity

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- DDR4 System SI requirement:
  - Rectangular mask for DQ bus **measured at DRAM ball**
  - no Mask definition for CA Mask (DDR3 like AC/DC based approach)
- DDR5 System SI requirement:
  - Rectangular mask for CA bus **measured at the ball**
  - Diamond shape stressed eye for Receiver test is closest what can be used as input Mask for signal integrity measurement. This is defined after DFE, so **on the silicon die** with well defined Jitter stress.
- LPDDR4
  - Rectangular mask for CA bus **measured at the ball**
  - Rectangular mask for DQ bus **measured at the ball**
    - At 4267 and a QDP/ODP package this does not make sense any more and a SI check at the RX is required for System verification
- LPDDR5
  - Hexagonal mask for CA bus **measured at the ball**
  - Hexagonal mask for DQ bus **measured at the ball**
    - **Even with DFE enabled the mask definition is at the ball, what is a bit strange**

(LP)DDR5 signaling
WCLK/DQS vs. DQ alignment during Write

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- While DDR4 still showed a well center aligned Write DQS2DQ alignment LPDDR4 started with non-matched packages and introduced a tDQS2DQ offset in the range of 200-800ps (multiple UI) that needs to be trained
- On top of this there is
  - A temperature dependency for the on-die DQS clock tree that need to be periodically retrained (DQS clock tree oscillator training)
  - a 30ps DQ2DQ offset allowed what requires a per pin training for each DQ
- LPDDR5 changed this to „WCK2DQI“ with HF and LF (high and low Frequency) up to 300-900ps delay with some defined VT (Voltage/Temperature) variation.
- DDR5 introduced a tRX_TDQS2DQ_skew and even with a DLL the system need to be periodically re-trained due to VT variation not compensated by the DLL!

LPDDR5 signaling
WCK(DQS) vs. DQ alignment during READ

- LPDDR5 WCK2DQO allowed delay range is 650ps – 1900ps (multiple UI) also with some defined VT (Voltage/Temperature) variation.
- DDR5 has a multi UI (up to 5 UI) DQS to DQ skew that is programmed into the MR.

Other Features

- There are several other Features that are too much for this document:
  - Details on Decision Feedback Equalizer
  - Several new trainings are introduced
  - ZQ calibration based on VOH rather than Ron
  - DQS output jitter definitions
  - CLK/WCK input jitter definitions
  - New Pre- and Postambles
  - New 2N-Mode feature
  - BER definitions
  - ….

More topics and details are covered in the seminar „Open the Black Box of Memory“

Interface signal description: Command address DDR3/4/5

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Symbol DDR3	Symbol DDR4	Symbol DDR5	Type	Logical Group	DDR3	DDR4	DDR5
CK/CK#	CK_t/CK_c	CK_t/CK_c	Input	CLK	Differential clock: Sampling of CCA signals on rising clock edge		
CKE	CKE		Input	Ctrl	Clock Enable: Rank based Power Down control		No CKE pin
CS#	CS_n	CS_n	Input	Ctrl	Chips Select: Rank selection for multi rank configuration		Additionally triggers PDE/PDX
ODT	ODT		Input	Ctrl	On Die Termination: Enables termination on DRAM **DQ**		DQ ODT by Non-Target ODT MRS config, ODT-CA new misc signal
	ACT_n	CA[13:0]	Input	CA	N/A	Activation CMD: Defines ACT command and allows usage of RAS_n/A16, CAS_n/A15, WE_n/A14 as row address	Addresses and commands are sent during multi cycle commands. Special bits: CID[3:0] to be found in CA5, 11, 12, 13 BA[1:0] to be found in CA6, 7 BG[2:0] to be found in CA8, 9, 10 AP in CA10 BC in CA5
RAS# CAS# WE#	RAS_n/A16 CAS_n/A15 WE_n/A14		Input	CA	Command: Select function according to truth table. In DDR4, A14-A16 are reused as additional row addresses		
	C[2:0]		Input	CA	N/A	ChipID: Selects chip inside 3D TSV stack	
BA[2:0]	BA[1:0]		Input	CA	Bank Address: Defines which bank in DRAM is accessed. For MRS it defines the written register		
	BG[1:0]		Input	CA	N/A	Bank Group: Selects bank group	
A[15:0]	A[17:0]		Input	CA	Address: Multiplexed for row/column access. In DDR4, A14-A16 reused as command for column access)		
A10/AP	A10/AP		Input	CA	Auto-Precharge: A10 reused for command access and defines for READ/WRITE if the DRAM executes the precharge automatically		
A12/BC	A12/BC_n		Input	CA	Burst Chop: A12 reused for column command and defines for READ/WRITE if the burst is chopped		
	PAR		Input	CA	N/A	Parity: Command address parity	

Interface signal description: Data signals DDR3/4/5

Symbol DDR3	Symbol DDR4	Symbol DDR5	Type	Logical Group	DDR3	DDR4	DDR5
DQS DQS#	DQS_t DQS_c	DQS_t DQS_c	IO	DQ	Differential data strobe: Source synchronous timing information for sampling data on DQ lines. For DRAMs x8/x16/x32 strobe per byte, for x4 DRAMs strobe per nibble		Differential data strobe: output with read data, input with write data
DQ	DQ	DQ	IO	DQ	Data query: data signals. Number according to DRAM organization: x4, x8, x16, x32		
DM	DM_n DBI_n TDQS_t	DM_n	Input*)***) IO**)	DQ	**D**ata **M**ask: mask selects bits inside a burst	**D**ata **M**ask / **D**ata **B**it **I**nversion / **T**erminate **DQS**: function selected by MRS. Some functions are dependent on organization.	Input mask signal for write data
TDQS TDQS#	TDQS_c	TDQS_t, TDQS_c	Output*)***) IO**)	DQ	Terminate DQS: used if x8 and x4 DRAMs are in the same system. Different implementation for DD3 vs. DDR4		Termination data strobe: applicable for x8 DRAMs only

*) DDR3
**) DDR4
***) DDR5 (tDQS as output is strange for DDR5)

Interface signal description: Supply and misc. DDR3/4/5

Symbol DDR3	Symbol DDR4	Symbol DDR5	Type	Logical Group	DDR3	DDR4	DDR5
VDDQ	VDDQ	VDDQ	Supply	Supply	DQ power supply: Between 1.1 V– 1.5 V depending on device (isolated on package from VDD)		
VSSQ	VSSQ	VSSQ	Supply	Supply	DQ GND		
VDD	VDD	VDD	Supply	Supply	Logic Power supply: Between 1.1 V – 1.5 V depending on device (isolated supplies on package)		
VSS	VSS	VSS	Supply	Supply	Logic and CA GND		
	VPP	VPP	Supply	Supply		Supply voltage for activation of DRAM wordline: 2.5 V	Supply voltage for activation of DRAM wordline: 1.8 V
VrefCA	VrefCA		Misc.	Misc.	Reference Voltage for Control/Command/Address (CCA)		
VrefDQ			Misc.	Misc.	Reference voltage for DQ		
ZQ	ZQ	ZQ	Misc.	Misc.	Reference pin for ZQ calibration		
Reset#	Reset_n	Reset_n	Input	Misc.	Reset: asynchronous signal for resetting the DRAM		
	Alert_n	Alert_n	IO	Misc.		Alert: output: CRC or Parity error flag input: for connectivity TM	Goes low when error in CRC occurs (for period time interval) Works as input during connectivity TM
	TEN	TEN	Input	Misc.		Connectivity TM enable: enables TM on x16 (optional on x4/x8)	Connectivity TM enable: required on x4, x8 and x16 devices

System VTT is termination voltage for CA on DDR3/4. This is not seen at the DRAM and therefore not included in the DRAM specification! For DRAM output characterization VTT is used as well.

Interface signal description: New misc. in DDR5

Symbol DDR5	Type	Logical Group	DDR5
MIR	Input	Misc.	To inform SDRAM device that it's being configured for mirrored or standard mode. When MIR pin is connected to VDDQ, SDRAM internally swaps even numbered CA with next higher odd number CA.
CAI	Input	Misc.	**C**ommand & **A**ddress **I**nversion: when CAI pin is connected to VDDQ, DRAM internally inverts logic level present on all CA signals. If no inversion is required, CAI pin must be connected to VSSQ.
CA_ODT	Input	Misc.	ODT for Command and Address. Group A setting if pin connected to VSS, group B setting if pin connected to VDDQ
LBDQ	Output	Misc.	Loopback Data Output: when loopback is enabled, it is in driver mode using default RON; when loopback is disabled, pin is either terminated or at HiZ.
LBDQS	Output	Misc.	Loopback Data Strobe: single ended strobe with rising edge aligned with loopback data edge, falling edge aligned with data center. When loopback enabled, it's in driver mode using default RON; when disabled, pin is either terminated or at HiZ.

Interface signal description: Command address LPDDR4/5

Symbol LPDDR4(x) *	Symbol LPDDR5	Type	Logical Group	LPDDR4(x)	LPDDR5(x)
CK_t/CK_c A/B	CK_t/CK_c A/B	Input	CLK	Differential clock: sampling of CA signals on rising clock edge	Differential clock, sampling of CA signals at **rising and falling** clock edge (CK_t), CS sampled at rising edge (don't care for falling edge), single-ended mode allowed to reduce power consumption at low frequencies
CKE A/B		Input	Ctrl	Clock Enable: rank based power down control	
CS A/B	CS_n A/B	Input	Ctrl	**C**hip **S**elect: rank selection for multi rank configuration (e. g. quad die packages)	
ODT_CA A/B		Input	Misc	Configures termination on DRAM **CA for LPDDR4 (not LPDDR4x), static signal!**	
CA[5:0] A/B	CA[6:0] A/B	Input	CA	Command Address bus Independent for Channel A and B Single data rate and multi cycle commands	Command Address bus Independent for Channel A and B Double data rate and multi cycle commands

* A/B indicates independent channels
Table describes dual channel only / Quad Channel with A/B/C/D is available too

Interface signal description: Data signals LPDDR4/5

Symbol LPDDR4(x)	Symbol LPDDR5	Type	Logical Group	LPDDR4(x)	LPDDR5(x)
DQS[1:0]_t A/B*) DQS[1:0]_c A/B*)	WCK_t A/B*) WCK_c A/B*)	IO **) Input ***)	DQ	Differential data strobe: source synchronous timing information for sampling data on DQ lines. For DRAMs x8/x16/x32 strobe per byte	Differential clocks used for write data capture, read data output. Single ended mode allowed during low frequency operations to reduce power consumption. For DRAMs x8/x16/x32 WCK per byte
	RDQS[1:0]_t A/B*) RDQS[1:0]_c A/B*)	Output/IO***)	DQ		Read data strobe: differential output clock signals to strobe data during read; RDQS_t also used as parity pin at write with link protection enabled. Single-ended mode for RDQS for low frequencies to save power.
DQ[15:0] A/B*)	DQ[15:0] A/B*)	IO	DQ	Data Query input/output: Bi-directional data bus	
DMI[1:0] A/B*)	DMI[1:0] A/B*)	IO	DQ	Combined data mask and data bus inversion (selected by MR setting)	Multiple functions (Data Mask, Data Bus Inversion, Parity) at read with EXX operation

*) A/B indicates independent channels
Table describes dual channel only / Quad Channel with A/B/C/D is available too
**) LPDDR4
***) LPDDR5: RDQS can be input pin when configured as Parity for link protection

Interface signal description: Supply and misc.

Symbol LPDDR4(x)	Symbol LPDDR5	Type	Logical Group	LPDDR4(x)	LPDDR5
VDDQ, VDD1, VDD2	VDDQ, VDD1, VDD2H/L**	Supply	Supply	Power supplies, isolated on die to reduce noises	
VSS VSSQ	VSS (VSSQ)*	Supply	Supply	Power supply GND reference	
ZQ	ZQ	Misc.	Misc.	Pin for reference resistor to calibrate output drive strength and termination resistance	Pin for reference resistor to calibrate output drive strength and termination resistance
Reset_n	Reset_n	Input	Misc.	Reset: asynchronous signal for resetting the DRAM	

*) VSSQ is not mentioned in Pad definitions, but later in the spec as GND reference for DataOut
**) VDD2H/L can be combined for high speed, or separated for Low Power (no DVFS used)