EKH DRAM eye evaluation routines

DRAM simulation evaluation
EKH .ael Code

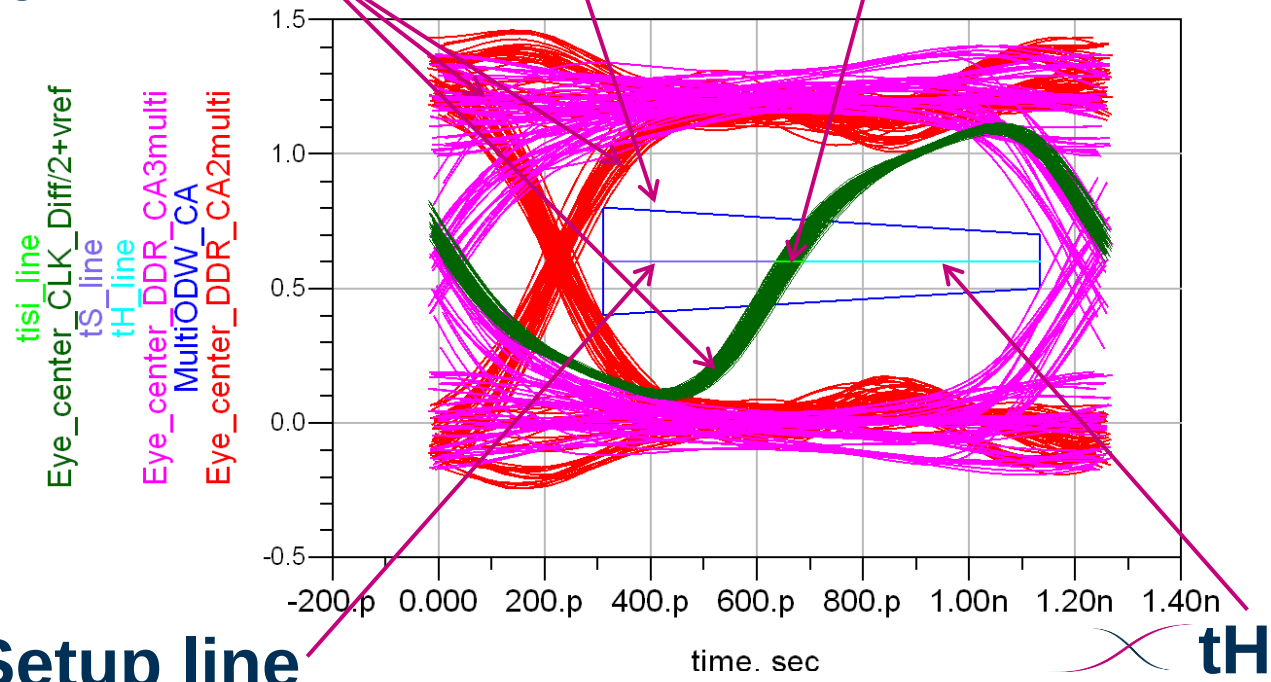
- **Intended for DDR2/3 Simulations**
  - AC/DC based Open Data window Calculation
  - ISI Calculation (Jitter at vref)
  - Tangential slew rate calculation
  - Multi-Open Data window
  - Multi-Net Delay calculation for delay based timing budgets
- **Includes the following functions**
  - Calculate and Draw Open Data window
  - Calculate and Draw ISI margin/line
  - Calculate and Draw slew rate value/line
  - Calculate and Draw setup/hold margin/line
  - Calculate and Draw delay to reference (incl. some TB calculation example)

Existing .dds Example: DDR2/3 ODW, Setup/Hold and ISI line

ODW: Multi Signal open Data Window

ISI line

Multiple Eyes incl. Timing Reference



tSetup line

tHold line

Existing .dds Example: DDR2/3 ODW, Setup/Hold and ISI lines

Eqn times_CA=EKH_multisignals_eyes_calc_DDR(signal_list, rate, vref, dAC,

indep(times_CA)	times_CA
Multi Valid Window[0]	822.4 p
Multi Valid Window End[1]	1.134 n
Multi Valid Window Start[2]	311.3 p
Multi Valid Window %[3]	65.79
Multi ISI[4]	351.8 p
Multi ISI End[5]	886.3 p
Multi ISI Start[6]	534.5 p
Multi ISI %[7]	28.14
Vref[8]	600.0 m
Vih ac[9]	800.0 m
Vih dc[10]	700.0 m
Vil ac[11]	400.0 m
Vil dc[12]	500.0 m
Delay of first Eye[13]	844.9 p

Eqn dly_CA3=EKH_eye_delay_DDR(Sig1,vref)

Eqn MultiODW_CA=EKH_gen_multieye_window_DDR(times_CA)

Eqn tS_line=EKH_gen_setup_time_line(tSH_CA)

Eqn tH_line=EKH_gen_hold_time_line(tSH_CA)

Eqn tisi_line=EKH_gen_isi_time_line(tSH_CA)

Eqn Eye_center_DDR_CA3multi=EKH_eye_center_DDR(Sig1,rate,vref,dly_CA3)

Eqn Eye_center_DDR_CA2multi=EKH_eye_center_DDR(Sig2,rate,vref,dly_CA3)

Eqn Eye_center_CLK_Diff=EKH_eye_center_CLK(Sig0_Diff,rate,vref,dly_CA3)

Eqn tSH_CA=EKH_calc_setup_hold_times_DDR3(rate,vref,dAC, dDC, times_CA, isi_DiffCLK, dly_CA3)

indep(tSH_CA)	tSH_CA
Setup time[0]	324.0 p
Hold time [1]	444.2 p
Diff Clock skew [2]	54.25 p
Valid window [3]	822.4 p
CLK skew start[4]	635.4 p
CLK skew end[5]	689.6 p
Valid window end[6]	1.134 n
Valid window start[7]	311.3 p
Delay[8]	844.9 p
vref[9]	600.0 m

Eqn isi_DiffCLK=EKH_calc_isi_diffCLK(Sig0_Diff, rate, vref, vref_diff, dAC, dDC

indep(isi_DiffCLK)	isi_DiffCLK
ISI[0]	54.25 p
ISI End[1]	689.6 p
ISI Start[2]	635.4 p
ISI %[3]	4.340
Vref[4]	600.0 m

Existing .dds Example
DDR2/3 Slew Rate Calculation

Calculate the slew rates for the weak and strong data signals and plot on the eye diagram

weak signals

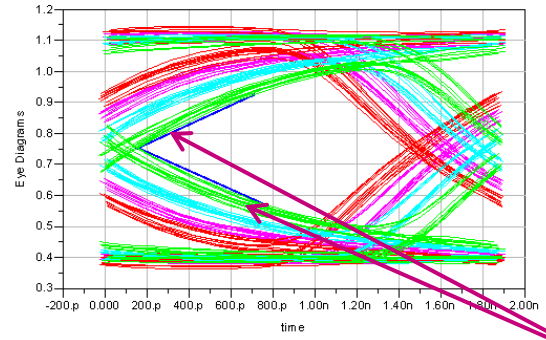
```
Eqn eyeH_W1=EKH_eye_isi_DDR(DramH1W,F,Vref_w,dly_w)
Eqn eyeH_W2=EKH_eye_isi_DDR(DramH2W,F,Vref_w,dly_w)
Eqn eyeH_W3=EKH_eye_isi_DDR(DramH3W,F,Vref_w,dly_w)
Eqn eyeH_W4=EKH_eye_isi_DDR(DramH4W,F,Vref_w,dly_w)

Eqn sr_W4=EKH_envelop_slew_DDR(DramH4W,F,Vref_w,del_ac,del_dc,dly_w)
Eqn Sr_Setup=max([sr_W4[0],sr_W4[1]])
Eqn W4_S_R=EKH_gen_envelop_slew_line_weak_rise_DDR(sr_W4)
Eqn W4_S_F=EKH_gen_envelop_slew_line_weak_fall_DDR(sr_W4)
Eqn signal_list=list(DramH1W,DramH2W,DramH3W,DramH4W)
```

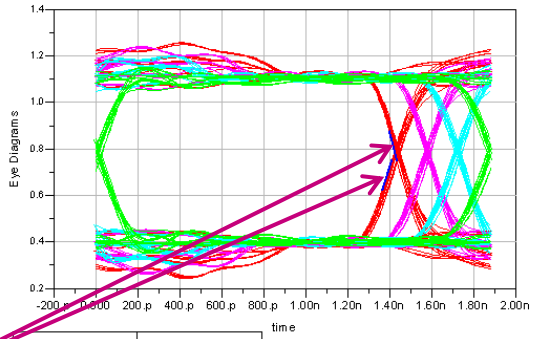
strong signals

```
Eqn eyeH_S1=EKH_eye_isi_DDR(DramH1S,F,Vref_s,dly_s)
Eqn eyeH_S2=EKH_eye_isi_DDR(DramH2S,F,Vref_s,dly_s)
Eqn eyeH_S3=EKH_eye_isi_DDR(DramH3S,F,Vref_s,dly_s)
Eqn eyeH_S4=EKH_eye_isi_DDR(DramH4S,F,Vref_s,dly_s)

Eqn sr_S3=EKH_envelop_slew_DDR(DramH1S,F,Vref_s,del_ac,del_dc,dly_s)
Eqn Sr_hold=max([sr_S3[2],sr_S3[3]])
Eqn S3_S_R=EKH_gen_envelop_slew_line_strong_rise_DDR(sr_S3)
Eqn S3_S_F=EKH_gen_envelop_slew_line_strong_fall_DDR(sr_S3)
Eqn signal_list1=list(DramH1S,DramH2S,DramH3S,DramH4S)
```



sr_setup_rising[0]	0.311
sr_setup_falling[1]	0.302



sr_hold_rising[2]	2.882
sr_hold_falling[3]	3.450

Multiple Eye in in one diagram incl. last and first slew rate lines

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Project Directory	Default Dataset Name	
F:/EKH/ADS/_Projects_2013/DRAM_Templates_wrk	CA_Sweep.ds	
Design Name	**Current time**	**Simulated**
DRAM_Templates_lib:_CA_SimulationExample:schematic	Fri Jul 12, 2013 16:55:08	Fri Jul 12, 2013 16:21:12

Disclaimer: Slew rates are calculated with the eye crossing centered. Due to this there are some limitations to plot them when the eye is centered. .ael code optimization should be possible!

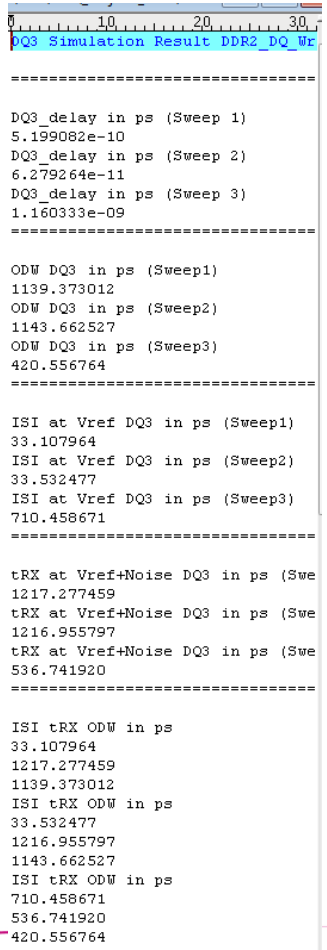
Evaluate “big” sweeps

.ael solution allows usage in schematic

- Simplest with ”Netlist Include”

ADS Schematic

Result Example



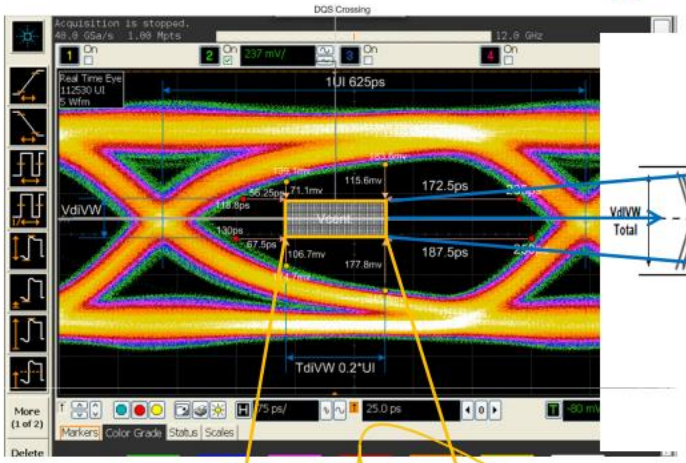
Netlist Example

```
; DQ3_Sweep2 Evaluation
aele dly_DQ3w_Sw2=EKH_eye_delay_DDR(DQ_3[2,::],Vref_Sim[0]);
aele EyeCenter_DQ3_Sw2=EKH_eye_center_DDR(DQ_3[2,::],DQ_BitRate_Sim[0],Vref_Sim[0],dly_DQ3w_Sw2[0]);
aele EyeISI_DQ3_Sw2=EKH_eye_isi_DDR(DQ_3[2,::],DQ_BitRate_Sim[0],Vref_Sim[0],);
aele ACDCtimes_DQ3_Sw2=EKH_calc_times_DDR(DQ_3[2,::],DQ_BitRate_Sim[0],Vref_Sim[0],dAC_Sim[0],dDC_Sim[0],);
aele Vreftimes_DQ3_Sw2=EKH_calc_times_DDR(DQ_3[2,::],DQ_BitRate_Sim[0],Vref_Sim[0],+0.01,-0.01,);
aele ISI_ps_DQ3_Sw2=ACDCtimes_DQ3_Sw2[4]*1e12;
aele tRX_ps_DQ3_Sw2=Vreftimes_DQ3_Sw2[0]*1e12;
aele ODW_ps_DQ3_Sw2=ACDCtimes_DQ3_Sw2[0]*1e12;
aele Values_DQ3_Sw2=[ISI_ps_DQ3_Sw2, tRX_ps_DQ3_Sw2, ODW_ps_DQ3_Sw2];
; aele ACDCtimes_DQ3_SwAll=EKH_calc_times_DDR(DQ_3[::,::],DQ_BitRate_Sim[2],Vref_Sim[2],dAC_Sim[2],dDC_Sim[2],dly_DQ3w[2]);
;
aele ZZZCreateDir3=mkdir(strcat(OutDir, SimDescription));
aele ZZZCreateSubDir_Sw0=mkdir(strcat(OutDir, SimDescription, "\\", Sweep0));
aele OutPath_Sw0=strcat(OutDir, SimDescription, "\\", Sweep0, "\\");
aele Export_DRAM_Parameters_Descr=write_var(strcat(OutPath_Sw0, "DQ3_Data.txt"), "W", strcat("DQ3 Simulation Result " , SimDescription) , " " , "f" , 1, Dumm
aele Export_DRAM_Parameters_Separator001=write_var(strcat(OutPath_Sw0, "DQ3_Data.txt"), "A", "==================================================" , " " ,
;aele Export_DQ3_Sw0=write_var(strcat(OutPath_Sw0, "DQ3_Data.txt"), "A", , ",", "s" , ,[Data_Collection_Start::Data_Output_Increment::Data_Collection_Stop],
aele Export_DQ3_Sw0_dly=write_var(strcat(OutPath_Sw0, "DQ3_Data.txt"), "A", "DQ3_delay in ps (Sweep 1)" , " " , "s" , , [dly_DQ3w_Sw0]);
aele Export_DQ3_Sw1_dly=write_var(strcat(OutPath_Sw0, "DQ3_Data.txt"), "A", "DQ3_delay in ps (Sweep 2)" , " " , "s" , , [dly_DQ3w_Sw1]);
aele Export_DQ3_Sw2_dly=write_var(strcat(OutPath_Sw0, "DQ3_Data.txt"), "A", "DQ3_delay in ps (Sweep 3)" , " " , "s" , , [dly_DQ3w_Sw2]);
aele Export_DRAM_Parameters_Separator002=write_var(strcat(OutPath_Sw0, "DQ3_Data.txt"), "A", "==================================================" , " " ,
```

DDR4 Outlook
JEDEC definitions

EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

Understanding the DDR4 Eye



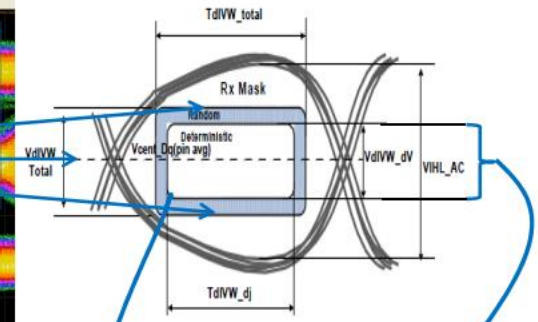


Figure 187 — DQ Receiver(Rx) compliance mask

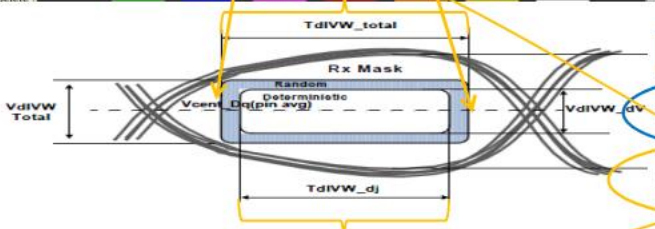


Figure 187 — DQ Receiver(Rx) compliance mask

Table 103 — DRAM DQs In Receive Mode; * UI=tck(avg)min/2

Symbol	Parameter	1600,1866,2133		2400		2666,3200		Unit	NOTE
		min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	136 (note12)	-	tbd	-	tbd	mV	1,2,4,6
VdIVW_dV	Rx Mask voltage - deterministic	-	136	-	tbd	-	tbd	mV	1,5,13
TdIVW_total*	Rx timing window total	-	0.2 (note12)	-	tbd	-	tbd	UI*	1,2,4,6
TdIVW_dj	Rx deterministic timing	-	0.2	-	tbd	-	tbd	UI*	1,5, 13

DDR4 eye mask specified for total jitter (Rj + Dj) and deterministic component (Dj)
BER <= 1e-16

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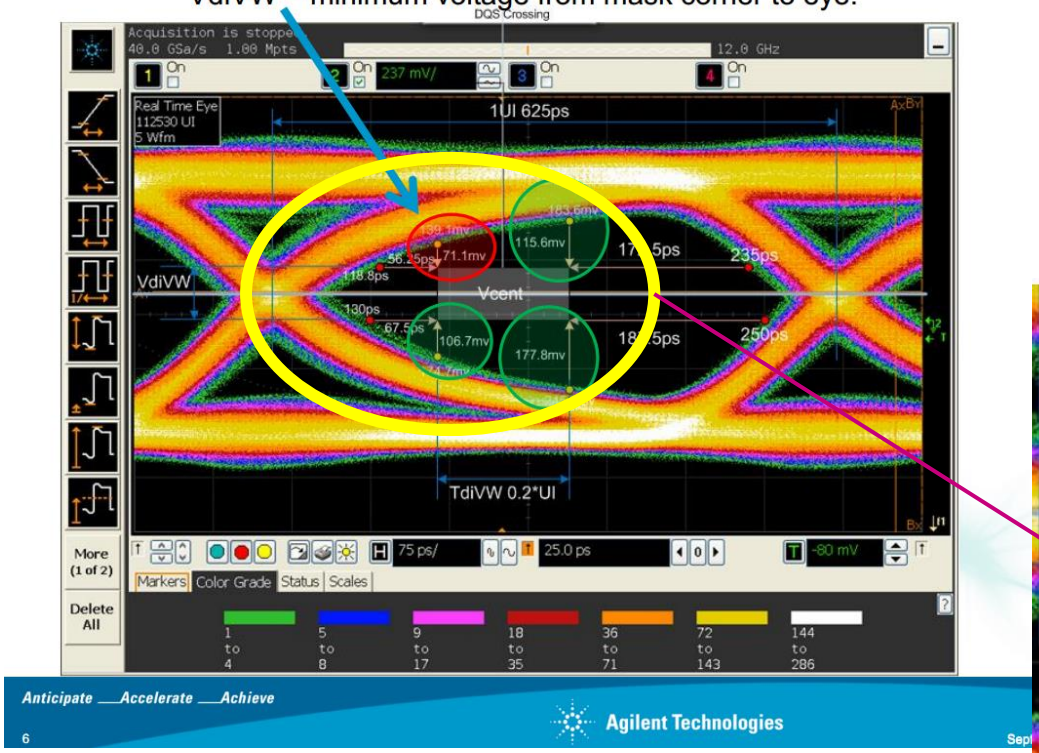
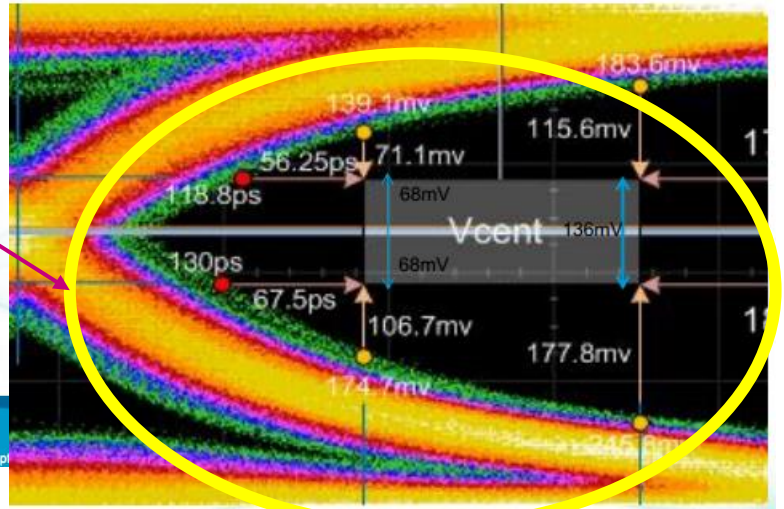
DDR4 Outlook
Measurement considering DJ

DDR 4 Eye Voltage Margin to Mask (up to 2133).

VdiVW = minimum voltage from mask corner to eye.





Voltage margin is measured analogously to timing margin:
Margin is then (139mv-68mv)/68mV * 100% =104%

DDR4 Outlook
Eye Mask considering RJ+DJ

Inside the DDR4 Eye

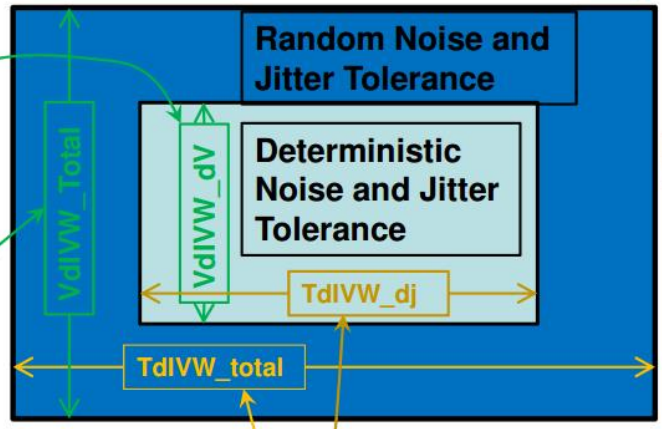


Table 1 -- Key Jitter Characterization Parameters

Parameter	Symbol	Min	Max	Unit	Note
Bit Error Ratio	BER				3,4

Table 103 — DRAM DQs In Receive Mode; * UI=tck(avg)min/2

Symbol	Parameter	1600,1866,2133		2400		2666,3200		Unit	NOTE
		min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	136 (note12)	-	tbd	-	tbd	mV	1,2,4,6
VdIVW_dV	Rx Mask voltage - deterministic	-	136	-	tbd	-	tbd	mV	1,5,13
TdIVW_total	Rx timing window total	-	0.2 (note12)	-	tbd	-	tbd	UI*	1,2,4,6
TdIVW_dj	Rx deterministic timing	-	0.2	-	tbd	-	tbd	UI*	1,5, 13

DDR4 eye mask specified for total jitter (Rj + Dj) and deterministic component (Dj)

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Current Spec status

Figure 199: Rx Mask to ^{t}DS/^{t}DH Conversion

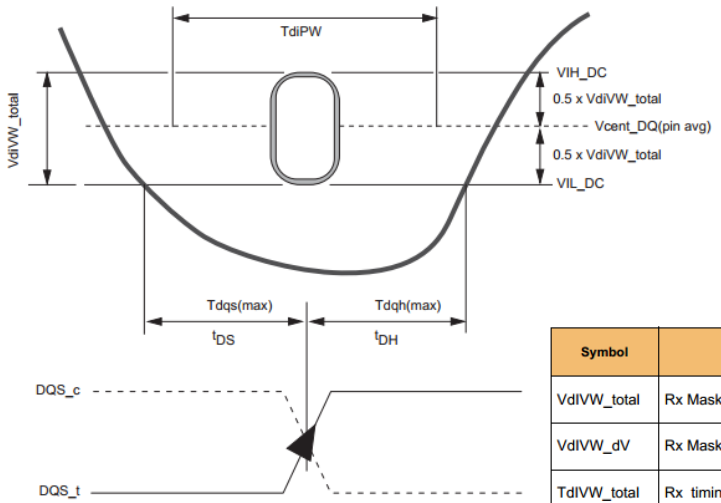

Table 103 — DRAM DQs In Receive Mode; * UI=tck(avg)min/2

Symbol	Parameter	1600,1866,2133		2400		2666,3200		Unit	NOTE
		min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	136 (note12)	-	tbd	-	tbd	mV	1,2,4,6
VdIVW_dV	Rx Mask voltage - deterministic	-	136	-	tbd	-	tbd	mV	1,5,13
TdIVW_total	Rx timing window total	-	0.2 (note12)	-	tbd	-	tbd	UI*	1,2,4,6
TdIVW_dj	Rx deterministic timing	-	0.2	-	tbd	-	tbd	UI*	1,5, 13
VIHL_AC	DQ AC input swing pk-pk	186	-	tbd	-	tbd	-	mV	7
TdIPW	DQ input pulse width	0.58		tbd		tbd		UI*	8
Tdqs_off	DQ to DQS Setup offset	-	tbd	-	tbd	-	tbd	UI*	9
Tdqh_off	DQ to DQS Hold offset	-	tbd	-	tbd	-	tbd	UI*	9
Tdqs_dd_off	DQ to DQ Setup offset	-	tbd	-	tbd	-	tbd	UI*	10
Tdqh_dd_off	DQ to DQ Hold offset	-	tbd	-	tbd	-	tbd	UI*	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	tbd	9	tbd	tbd	tbd	tbd	V/ns	11

CA Specification Example

Same concept as for DDR3

Table 137: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter		Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
CMD, ADDR setup time to CK_t, CK_c referenced to $V_{IH(AC)}$ and $_{VIL(AC)}$ levels	Base	^{t}IS	115	–	100	–	85	–	65	–	ps	
	V_{REFca}	$^{t}IS_{VREF}$	215	–	200	–	185	–	165	–	ps	
CMD, ADDR hold time to CK_t, CK_c referenced to $V_{IH(DC)}$ and $_{VIL(DC)}$ levels	Base	^{t}IH	140	–	125	–	105	–	87	–	ps	
	V_{REFca}	$^{t}IH_{VREF}$	215	–	200	–	180	–	162	–	ps	
CTRL, ADDR pulse width for each input		^{t}IPW	600	–	535	–	480	–	435	–	ps	

Conclusion

- **DDR2/DDR3 functions are existing a .ael code**
- **Existing functions for Timing and Voltage margins from mask can be adjusted to DDR4**
  - CA should be straight forward
  - DQ bus will require some adjustments, but much existing functionality can be re-used!
- **Transient simulation is required for the existing ael code**
  - An adaption to Channel statistical simulations might require more change (need more detailed check on this one).
  - For DJ effects transient simulation should be OK
    - RJ effects can be considered in eye mask.
- **There will be some questions/decisions to be made**
  - E. g. Where to locate the Mask in the eye ?
    - Optimized for Timing or voltage (depends on Controller Training algorithm).