Memory compliance Testing and related services

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1 Revision History

Date	Rev.	Author	Chapters affected	Remarks
2019-07-27	0.01	Hermann Ruckerbauer	All	New Release, updated several times during working phase.
2019-09-02	0.02	Hermann Ruckerbauer	All	Minor typo correction
2020-01-19	0.03	Hermann Ruckerbauer	All	Adding DDR5/LPDDR4 Minor corrections
2020-05-25	0.04	Hermann Ruckerbauer	All	Minor corrections
2021-01-29	0.05	Hermann Ruckerbauer	All	Minor corrections

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2 Preface

Memory compliance testing is a complex task. There is no exact specification that exactly defines how this needs to be done! Validating a Memory interface is a task of engineering work and judgement.
EKH is having a lot of experience in running such verifications, but this does not guarantee that all issues will be found.
It is not possible to measure all signals. In this document EKH is recommending some selected signal combinations to be verified!
Dependent on the task it is required to do some rework (e. g. assembly of the interposer) and soldering on the DUT. Therefore, there is a chance that the DUT is going to be damaged. This is just a worst case scenario, but need to be mentioned!

3 Prerequisite and other information

The customer is responsible for several things to ensure that the measurements are possible and most effective.

3.1 Use of interposer

EKH strongly recommends to use an interposer to get access to test points for SI verification. It is also possible to measure at other testpoints (e. g. on vias at the backside of the PCB), but this requires to consider the location of the testpoint for evaluation of the measured data. For READ verification this might be required anyhow.
Whether the EKH interposer or any other interposer is used depends on the specific requirements. Even if EKH gets access to the Layout data, **it is the responsibility of the customer to ensure mechanical compatibility of the board with the selected interposer!** Especially assembly of the interposer is a difficult task and many assembly companies have problems to do this reliable! EKH has a very experienced assembly service provider but still it is strongly recommended to use 2 board for interposer assembly in order to have a backup in case one is not working. EKH can not guarantee that assembly of the interposer is working and there is even the risk that the board is damaged as for all soldering/re-work tasks! Even in this very unlikely case EKH the assembly need to be invoiced.

3.2 Memory test software

There is no specific JEDEC requirement for the testpattern that is used for the measurement. The more transitions one can get, e. g. in 50us timeframe, the more meaningful the test results are.

One of the most critical things during memory compliance testing is the READ/WRITE separation. It is preferable to have the option to run only READ or only WRITE accesses to the DRAM!
For x86 based CPU (e. g. Intel/AMD) PassMark Memtest86 is available and a good option to run e. g. the “Random Value” test to get random test data.
Another option is e. g. SMtest by Daniel Mysliwitz, which also allows to create own testpatterns.
For many other CPUs that can run linux (e. g. TI or nxp ARM based Controllers) “memtester 4.5.0” is a reasonable solution. Starting from version 4.3.0 allows to select a single test and run only single pattern. This works usually quite well, but has the disadvantage that the “Stuck Address” test is always executed, independent of the selected test pattern. Therefore, it is recommended to adjust the test and disable the “Stuck Address” test for memory measurements. The source code and binary are available at www.pyropus.ca!

3.3 Latencies: CL and CWL

it is required that the customer delivers the configured CL and CWL. Even with this information, sometimes it is not possible to perfectly separate bursts to different ranks or bubbles between bursts.

3.4 Settings for drive strength and termination

Standard verification measurements are executed expecting that it is only required to verify the configured drive strength and termination setting.
There might be other parameters of the output drivers that can be configured (especially in the controller). E. g. some controllers allow to adjust slew rate settings.
DDR5 will require equalization emulation in addition. For this new DRAM generation it is still to be investigated how this will be considered during measurements.
The customer should have selected the right values already, e. g. based on simulations, reference board design similarities or engineering judgement!
If possible, EKH will try to verify some different settings for such parameters, but a real optimization of the parameter is not included in the standard packages available. **Such optimization depends on the efforts that will be required and cannot be offered as lumped sum quote.**

3.5 Consideration of training

Different controllers will run different types of trainings during power up. Some controllers will be preconfigured by register settings, others will run trainings at each power up and some will only run trainings when they detect changes in the memory configuration.

It is the responsibility of the customer that the system status during verification is similar to the normal usage case.

3.6 Compliance app result judgement

Every system does show different signal integrity. It is not possible to guarantee that all measurements can be executed as planned. Especially the compliance apps often run into trouble (e. g. due to READ/WRITE separation). EKH checks the compliance reports based on experience and engineering judgement. Sometimes tests are PASS, but actually are FAIL, other tests are FAIL, but are just measured wrong and should be PASS.
The DRAM spec is not written in order to be verified in the system and therefore there are many things not really well defined. EKH has the experience to check the results of the compliance tests based on engineering judgement. It is possible that the final report of the scope vendor shows FAIL, but EKH judges this as “PASS” or don’t care!

3.7 Test content

The standard test setup considers only the most important tests at room Temperature.
Tests at different temperature need to be ordered separately.
Test that can performed by customer with standard desing KnowHow are not included as well. E. g. Power ramp or sequence measurements are not included in the normal package and would need to be ordered separately
Read tests

4 EKH services

4.1 Signal integrity (SI)

4.1.1 Interposer Assembly

This is not really a signal integrity based service, but a prerequisite for the measurements below. The service is bound to EKH interposers, but can be offered for other vendors interposer as well. Assembly of interposers is a rework process and therefore EKH cannot guarantee that it is working on the first try! EKH is working with a very experienced assembly house and the yield of re-work is really high! Standard procedure is that the customer delivers new DRAMs that can be used, but it is also possible to desolder the older DRAM, clean and reball it and use it again. This is often required for DIMMs, where it

is difficult to get the same DRAM again. Of course this increases the risk of a failure and can lead to degradation (mainly in the Array, decreasing refresh times) of the used DRAM. The customer needs to ensure mechanical compatibility of the interposer with his Layout based on the User Guide of the interposer. For LPDDR4 and DDR5 there are liftup PCBs available that increases the allowed height for surrounding components. Alternative to the lift up PCB is a socket solution that allows to click in DRAMs or re-balled interposers.

4.1.2 Command Address Signal Integrity verification

For most DDR memory the Control/Command/Address bus works at a lower frequency, but still this is one of the most critical busses due to the Point to Multipoint connectivity (e. g. FlyBy bus for DDR3/4).
In addition, different signals might have different loads and therefore timing adjustment is required for the different signals. This includes CLK/Control/CA signals.
Recommended is to verify at least CLK and CS (if Control and CA are identical configured and routed).
Several controllers do not drive the Command bus as long as CS is not active. For such systems it is recommended to verify at least one CA signal as well. Usually lower addresses (but high enough not to select the start bit of a burst) are switching quite often and are therefore good candidates for measurement.
But in any case, selection of specific addresses should consider a short layout check whether there is any worst case that should be measured (e. g. shortest, longest signal routing or the signal with the most crosstalk or the worst case via configuration).
Sometimes controller even use power down modes with CKE during memory test. When CKE is used, the controller can set CS into tristate as well! So far none of the scope vendors compliance apps do support verification with tristate on CA bus. It is possible to disable such power save features, but of course then the measurement does not represent the normal usage case anymore!

In case of a flyby bus implementation (e. g. DDR3/4) or some asymmetric CA branches each DRAM will get different input signal quality. E. g. CLK as steady state signal will get different levels dependent when all the reflections from the bus hit the specific DRAM location.
Usually the first (or second) DRAM in the Flyby bus chain is getting the worst case signal quality and therefore this is the most important DRAM to verify. Usually it is too much work to verify all DRAM positions, but EKH recommends to verify at least a second DRAM position, and there somehow towards the end of the bus. This will at least give a second datapoint and allows to see CLK to DQS alignment that is trained during Write leveling at two distant points of the flyby bus.

If required, EKH will use de-embedding, e. g. for the interposer or if the testpoint is too far away from the DRAM. EKH tries to limit this kind of postprocessing, as the error will get bigger the more de-embedding needs to be done. If a test fails, EKH will check if de-embedding is required. But usually when using an interposer it is more important to fix the design rather than trying to get a pass by de-embedding (or find some holes in the specification).

EKH uses eye measurements as well as scope vendors compliance app verification to verify CA signal integrity! For eye measurement EKH might use scope vendors tools supporting functionality:

- Zone Trigger with infinite persistence (Keysigth / Rohde&Schwarz)
- RTE with gating function (Keysight)
- DDR Debug Tool (Keysight)
- DDR-Debug (LeCroy)
- DDR eye (Rohde&Schwarz)

Which tool or method is used for eye measurement depends on the vendor and on the system behavior!

Most scope vendors state that their tools are used to validate the JEDEC DRAM specification with Command Address tests. This is not really true!
The DRAM spec is a device spec and in order to verify the CA input of the device it is required to put the DRAM on an ATE tester, apply the minimum input timings and verify the DRAM is still able to recognize the signals correctly!
This is the task of the DRAM vendor and most EKH customers are not interested in verifying the DRAM (they rely that this was done by the DRAM vendor), but they want to verify their system implementation!
And this is implemented in the scope vendors tool suites: Measure the signals and verify that they are better than required by the DRAM spec!

4.1.3 DQ Write

DQ write verification measurement is the standard measurement that most customers look for. In order to run this verification, it is required to separate READ and WRITE bursts. Especially for multi ranks systems it is important also to separate accesses to the different ranks by CS and only verify the accesses to the given rank. Write Leveling verification is included in this measurement.
If the DUT (Device Under Test) uses DIMMs, it is required to test different population configurations. Worst case is a fully populated configuration with the maximum number of DRAMs, but the configuration with lightest load should be also verified.

Similar to the CA bus, EKH uses eye measurement to check signal quality of the DQ write. De-embedding is handeled similar used as described for the CA bus!

Most scope vendors state that their tools are used to validate the JEDEC DRAM specification with DQ WRITE tests. This is not really true!
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4.1.4 DQ Read

DQ Read verification is much more difficult. The memory DQ bus is bidirectional, but due to packages, different drivers, different loads and terminations at both ends it is not symmetrical. It is required to measure READ at the controller input and validate the signal quality against the controller input spec. As the controllers are no commodity products with a common base spec (like the JEDEC DRAM spec), each controller requires unique verification!
In addition, the controller packages usually are large compared to the DRAM packages and de-embedding is always recommended (independent on whether the Controller spec defines the input signals at the ball or at the die).

Due to this fact the READ verification is not part of standard packages available from EKH. Detailed READ verification depends on the required efforts.
EKH will look to the READ signal at the DRAM and will try to do some judgement based on experience.

Most scope vendors state that their tools are used to validate the JEDEC DRAM specification with DQ READ tests. This is really true when validating the DRAM output signal! **But this is not what System designers would like to check.**
Most EKH customers are interested in system verification and this is not supported by the DRAM compliance apps!
For DRAM output verification it is required to put the DRAM on a special testboard and often special testmodes are required. Usually only DRAM vendors are capable of doing a solid DRAM output verification test.

EKH disables all READ tests in the compliance app for System verification as they are meaningless anyhow!

4.1.5 Optimization of DriveStrength and Termination

Optimization of Drive Strength and termination for WRITE depends on Controller configuration and training sequences. Due to this fact it is not possible to provide a lumped sum quote for this task, but such projects need to be calculated based on efforts.
For READ this is even more critical due to the difficulty with de-embedding and missing testpoints/interposer at the controller.
For multi rank systems (e. g. with several DIMMs) the complexity increases with every additional rank that needs to be considered.
For CA this is also valid and this might need to include soldering of termination resistors.
Optimization of Drive Strength, Termination, Slew Rate (and other) settings is only available based on efforts used.

4.1.6 CKE and Power Down timings

From a signal integrity perspective CKE is a control signal and can be expected to be similar to CS!
Power down timings (entry and exit) are not part of standard signal integrity verification measurements. Some systems/controllers utilize CKE extensively and especially in such cases it is recommended to verify CKE timings as well. This does not only include checking of signal integrity of CKE but also special timing verifications.
Verification of CKE and Power Down timings is only available based on efforts used.
Power Down timings are often verified in case issues with S3 wake are observed.

4.1.7 ODT timings

For signal integrity ODT is a control signal and in most cases can be expected to be similar to CS!
Issues with ODT timings are often seen in WRITE/READ measurements (e. g. Termination is switched on too late or too early). For READ the controller uses internal timings to enable ODT and therefore this is even more difficult to analyze.
Verification of ODT signal and timings is only available based on efforts used.

4.1.8 Vref/Power noise measurement

Power and Vref noise are difficult to measure and judge as the spec is not really clear on the parameters (e. g. bandwidth of measurement is not defined). EKH will measure Power and Vref noise at a capacitor as close as possible to the DRAM. Both signals are

measured against GND. Only for special analysis EKH will e. g. measure Vref referenced to VDD/2.
Standard power/Vref noise will be measured with different measurement bandwidth and evaluated based on engineering judgement.

4.1.9 Vref margin test

If the design was done considering DFT (Design for Testability) and allows a Vref margin test, EKH can executed this test as well. This test is strongly recommended and can also be executed by the system designer. Usually this is possible, when a voltage divider is used to generate Vref. During a memory test Vref is changed until memory fails occur. This test uses the DRAM out of spec and the result is evaluated based on EKH engineering judgement!

4.1.10 Signal integrity at different temperatures

The standard test is executed at room temperature. **Signal integrity measurements at specific temperatures can be offered, but are invoiced based on required efforts!**

4.1.11 Simulation service

Any Design can also be checked by simulations, e. g. S-parameter extraction or transient simulation. Such services cannot be offered as lumped sum, as every design is different and it depends on the target which simulation is actually required. Most likely, simulation service cannot be offered as lumped sum quote for any first project. For follow up projects it might be possible, but need to be discussed on a per project basis.

4.2 Other signals, Digital timings and miscellaneous

4.2.1 Reset signal quality and timing

Reset signal is an asynchronous signal and usually not verified in standard memory verification measurements.
EKH can support Reset verification, but this is only available based on efforts used.

4.2.2 ECC verification

ECC verification can be quite difficult and requires access to controller specification, datasheets and tools. **EKH can support ECC verification, but this is only available based on efforts used.**

4.2.3 CA parity and Alert verification

This is even more difficult than DQ bus ECC verification as simple measures like shorting a single DQ line is not possible here.
Verifying the Alert signal quality requires inducing a CA parity fail, what is only possible using special controller features.
EKH can support CA parity and Alert verification, but this is only available based on efforts used.

4.2.4 Clock frequency changes

Some controllers change clock frequency dependent on the traffic on the memory interface. For commodity DDR this is not that often used, for LPDDRx this is a standard usage model. Each frequency should be verified independently! The minimum required is the highest frequency, but it is also possible that the worst case is at the lower frequency. The digital timings will change based on the interface speed and should be verified as well. The customer is required to provide a setup where a fixed frequency is set that allows to measure without having the system switching between different frequencies.
Basically, each verification frequency requires to order the requested measurements independently, but will get a discount as no new physical setup is required.

4.2.5 Schematic review

A schematic review is recommended for every memory verification measurement. This helps EKH to understand the system and adjust the test strategy if needed. If the customer provides the schematic as .pdf, a short review is included in the base package that is ordered. This is not replacing a full Design/Layout review.

4.2.6 Layout review

A layout review is recommended for every memory verification measurement. This helps EKH to understand the system and adjust the test strategy if needed. E. g. by this EKH might select specific signals for testing.
If the customer provides the layout (best as ODB++) a short review is included in every base package that is ordered. This is not replacing a full Design/Layout review.

4.2.7 Full Design and Layout review

A full Design/Layout review (including check of Stackup/Material) can be ordered as well, but **it depends on the system complexity whether this can be quoted as lumped sum or based on real efforts. A first data check is required in order to write a quote for such a task.**

4.2.8 Digital timing verification

Digital timing verification is usually done by the logic analyzer. Whether it is required strongly depends on the controller used. If the system designer needs to program registers for configuration it is strongly recommended that at least a quick check of the most important digital timings is executed during memory interface verification.
EKH will try to identify the most important timings based on CS switching and other measurements. But it cannot be guaranteed that the minimum timings are actually found!
Timings that are checked are: CL, CWL, tRCD, tRP, tREFI, tRCD and OCD (Off Chip Driver) ZQ calibration frequency. An extensive verification of protocol with a logic analyzer is possible, but will be quoted based on real efforts.

4.2.9 Evaluation of controller training results

All controllers today run complex trainings during Power up or for one time configuration. Every controller is different and needs individual treatment. EKH has quite some experience, e. g. in manually decoding log files, but this cannot be offered as lumped sum quote.
Verification of controller training results is only available based on efforts used.

5 Available lumped sum packages

All the above services can be provided by EKH, but often it is not possible to provide a lumped sum quote and work need to be invoiced based on real efforts. But some lumped sum packages are available.

5.1 Base Package:

This is the smallest package and minimum to be ordered:
Single Rank system verification with CLK, DQS, DQ, CS measured with compliance test app and manual data eye check. Read eye is captured at the DRAM and therefore might suffer from reflection due to the testpoint at the DRAM. EKH will use engineering judgement to get a rough understanding whether the READ eye at the controller looks reasonable! Interposer Assembly need to be ordered separately. The base package needs to be ordered for every DRAM position that should be verified.
Order number: 401100

5.2 Additional CCA signal verification

Additional **C**ontrol, **C**ommand or **A**ddress signal. For multi rank systems (Control are different to CA signals) or Systems with tristate on CA this is recommended.
This can be ordered for as many signals as required as long as the used interposer provides access to the signals (the EKH interposers allow to access (nearly) all signals).
Order number: 401101

5.3 Additional DQ signal verification

Measurement of other DQ signals for WRITE verification. READ is verified with the limitations mentioned above!
This can be ordered for as many signals as required as long the used interposer provides access to the signals (the EKH interposers allow to access (nearly) all signals).
Order number: 401102

5.4 Power noise measurement

Power noise measurement as described above.
Order number: 401103

5.5 Vref margin test

Vref margin test as described above.
Order number: 401104

5.6 Digital timing verification

Check of digital timings based on CS as mentioned above
Order number: 401105

5.7 DRAM interposer assembly

Assembly of interposer with delivery of a new DRAM (DDR2/3/4)
Order number: 401106

Assembly of interposer with re-use of old DRAM (DDR2/3/4)
Order number: 401107

Assembly of interposer with delivery of a new DRAM DDR5 / LPDDR4
Order number: 401108

5.8 Check at additional Clock frequency

For any ordered “Base package” or other service a check at additional clock frequency can be ordered at a discount price
Order number: use the one shown above, just add “_2ndFSP”.
Example order number for the base package at a second Frequency set point: 401100_2ndFSP

6 Services that are not possible to quote as lumped sum quote

Some things like Design and Layout review for complex designs need to be invoiced based on an hourly basis for real efforts. For such things EKH recommends to define some upper limit for the budget. This can be used flexible to start working and identify the efforts needed. During this start up phase the customer can judge if EKH can really help. The customer can decide either to stop the project or extend the budget.
For such a setup EKH can quote for pure consulting service. If simulation tools (e. g. ADS) or Measurement tools (Scope, VNA, TDR, …) are required the hourly rates will be dependent on the required hardware.