

WHAT YOU ALWAYS WANTED TO KNOW ABOUT MEMORY! ... BUT NEVER HAD THE RIGHT EXPERT TO ASK!

OPEN THE BLACK BOX OF MEMORY

June 21./22. 2018 Cost: 1.700\$ (excluding VAT)

You are developing hardware e. g. for an "Embedded Computer System"?

It's a don't care for which processor platform: DRAM Memory is part of nearly all Designs. But the functionality behind the memory is often unknown. The layout is done following the design guide. But without some background KnowHow it is difficult to judge what impact required deviations from the design guide will have! The BIOS to access the memory is taken from the CPU vendor, without the

Date



DRAM X-ray - Get a clear view

possibility to look inside or even make adjustments. This makes troubleshooting quite difficult.

The memory interface is getting more and more a "Black Box"! With every new memory generation the margins are getting smaller and the requirements for the design are increasing. Get the KnowHow for designing successful products in the future.

DDR2 Address-

and Databus

Routing

Seminar content:

- » DRAM inside: What's inside the components?
- » Basic commands: How to access the DRAM?
- » ECC: How does it work and how to test it?
- » Specification
 - AC/DC: "Highway to Hell" ? Alternating Current / Direct Current?
- Derating ... ?
- » Application Test for Memory
- » SPD Content
- » Routing and Layout: Real world implementation
- » DDR2 vs. DDR3 vs. DDR4: The most important differences!
- » Signal Integrity: How to simulate signals?
- » Power Integrity: Can the components be supplied with current?
- » S-Parameter: How to read data in the frequency domain?
- » Compliance Test

The next seminar is in english language, for german or other locations just contact us directly!

Location: Plese see our website for details!

Detailed Information and Registration on www.EyeKnowHow.de

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EyeKnowHow: Your Key to "High Speed Signaling" KnowHow

The verification of logic functionality is not enough for today's products. "High Speed Digital" data transfer is not digital any more. Parasitic effects can distort the signals already at frequencies as low as 100MHz in a way that the receiving chip cannot recognize any more if a "0" or a "1" was sent.

The rising datarates on serial and parallel interfaces in each new generation increases this effect exponentially. The margins for data transmission are decreasing in the same degree. Don't care if PCIexpress or DDR2/3 – it gets more and more difficult to ensure the functionality of an electronic device under all circumstances. The solution to take only best of the best technologies is quite expensive. Materials with good electrical properties, blind vias or backdrilling provide high performance – but only at high cost. EyeKnowHow helps to select the right technology to achieve the required performance at limited production cost.

Would you like to meet us?

Visit us...

- ... at our booth on Embedded World 2019 Nuremberg - February 26.-28. 2019
- ... on our DRAM Seminar June 20./21. 2018 in Santa Clara

"DRAM-KnowHow - Open the Black Box of Memory"

The required technologies can be defined already during the design phase by simulations. You as customer don't have to invest in own expensive simulation tools. EyeKnowHow can also provide the development of critical designs. We do have special KnowHow in Memory interfaces directly from the DRAM development and can answer questions to DRAM internal functionality or the interface and it's physical implementation.

In addition we can offer fast and competent failure analysis. Dataeyes are our business, not just simulated, but also measured. Especially for memory interfaces we use our own tools for characterization and failure analysis.

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