EKH – EyeKnowHow

Signal Integrity made in Germany

WHAT YOU ALWAYS WANTED TO KNOW ABOUT MEMORY…
… BUT NEVER HAD THE RIGHT EXPERT TO ASK!

DRAM KnowHow

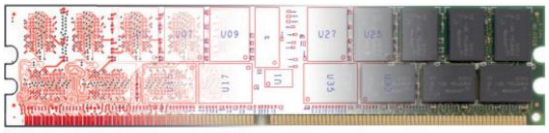
OPEN THE BLACK BOX OF MEMORY

19.02-21.02.2024 in Copenhagen
26.02-28.02.2024 in Munich
Cost: 2.400 Euro (excluding VAT)

You are developing hardware e. g. for an "Embedded Computer System"?

It's a don't care for which processor platform: DRAM memory is part of nearly all designs. But the functionality behind the memory is often unknown. The layout is done following the design guide. But without some background KnowHow it is difficult to judge what impact required deviations from the design guide will have! The BIOS to access the memory is taken from the CPU vendor, without the possibility to look inside or even make adjustments. This makes troubleshooting quite difficult.

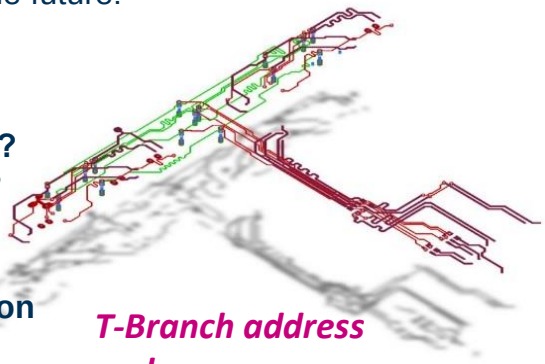
The memory interface is getting more and more a "Black Box"! With every new memory generation the margins are getting smaller and the requirements for the design are increasing. Get the KnowHow for designing successful products in the future!



DRAM X-ray - Get a clear view

Training content:

- **DRAM inside: What's inside the components?**
- **Basic commands: How to access the DRAM?**
- **Specification**
- **Application and compliance test for memory**
- **Routing and layout: Real world implementation**
- **DDR3 vs. (LP)DDR4: What's the difference?**
- **DDR5/LPDDR5: Whats new ?**
- **Signal integrity: Simulate your design!**
- **Power integrity: Improve your PDN design!**
- **S-Parameter: Read data in the frequency domain!**



T-Branch address and P2P databus routing

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Details and Information
www.EyeKnowHow.de

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EyeKnowHow: Your key to „High Speed Signaling“ KnowHow

The verification of logic functionality is not enough for today’s products. “High Speed Digital” data transfer is not digital anymore. Parasitic effects can distort the signals already at frequencies as low as 100 MHz in a way that the receiving chip can not recognize anymore if a “0” or a “1” was sent. The rising data rates on serial and parallel interfaces in each new generation increases this effect exponentially. The margins for data transmission are decreasing in the same degree. Don’t care if PCI express or DDR2/3 – it gets more and more difficult to ensure the functionality of an electronic device under all circumstances. The solution to take only best of the best technologies is quite expensive. Materials with good electrical properties, blind vias or backdrilling provide high performance – but only at high cost. EyeKnowHow helps to select the right technology to achieve the required performance at limited production cost.

Would you like to meet us?

Visit us …

... in our DRAM Trainings Feb. 2024

... at DesignCon 2024 (Santa Clara, US)

... at Embedded World 2024 (Nuremberg, Germany)

The required technologies can be defined already during the design phase by simulations. You as customer don’t have to invest in own expensive simulation tools. EyeKnowHow can also provide the development of critical designs. We do have special KnowHow in Memory interfaces directly from the DRAM development and can answer questions to DRAM internal functionality or the interface and its physical implementation. In addition we can offer fast and competent failure analysis. Data eyes are our business, not just simulated, but also measured. Especially for memory interfaces we use our own tools for characterization and failure analysis.

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