EYE KNOW HOW
HIGH SPEED SIMULATION AND MEASUREMENT

Open the Black Box of Memory

Content

Open the Black Box of Memory Overview

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- **The 2 day Seminar "Open the Black Box of Memory" provides a detailed view for design, layout and test engineers working with DRAM**
- **The focus is on DDR4 based on the changes from previous generations. This allows an easy transition for engineers knowing DDR2/3 to DDR4**
  - Nevertheless many things are very similar for the different generations
- **Even the course is already detailed for many topics there would be even more details available.**
  - This level of detail will be only interesting for a very limited amount of people and everybody would be interested in different topics.
  - If you need more insight in some special features please contact EyeKnowHow directly.

Open the Black Box of Memory
Agenda Part 1

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1. Seminar Target and Overview
2. Different Applications and Memories
3. DRAM Basics: DDR2/3/**4** Commands, Pins, Array
4. Evolution of commodity DRAM generations DDR2/3/**4**
5. Memory System Performance
6. DDR2/3/**4** Spec: Input Timings and Currents
7. DDR2/3/**4** Spec: Setup/Hold Derating
8. Timing Budget Calculation
9. Different DIMM Types and physical implementation
10. Setup for flexible module density

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Agenda Part 2

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1. Error Correction
2. Layout Guidelines
3. Measurement and Equipment
4. TDR Measurement
5. Failure Analysis
6. Transient Simulation
7. PDN Simulation
8. S-Parameter
9. Rules of Thumb and some Theory
10. Backup

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Agenda Part 3

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1. Overview on Training options
2. Power Up Sequence and „Low speed signaling“
3. ZQ Calibration
4. CA bus Calibration (per CA bus or per bit)
5. Write Leveling
6. Write DQS/DQ timing alignment (per byte or bit)
7. Receive Enable Training via MPR
8. Read DQS/DQ timing alignment (per byte or bit)
9. DDR4 “VrefDQ Training”