EYE KNOW HOW
SIGNAL INTEGRITY MADE IN GERMANY

Open the Black Box of Memory

Content

Open the Black Box of Memory Overview

- Goal: Provide detailed view for design, layout and test engineers working with DRAM
- Duration: 2 to 3 days (dependent on seminar format)
- The focus is on (LP)DDR4/5 based on the changes from previous generations. This allows an easy transition for engineers knowing DDR3 to DDR4/5 and LPDDR4/5 memory.
- High level of detail for many topics, On the fly selection of topics that should be discussed more intensively
  - If a very close insight into some special features is required, please contact EyeKnowHow directly

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Agenda part 1

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1. Seminar target and overview
2. Different applications and memories
3. DRAM basics
4. Evolution of commodity DRAM generations
5. Memory system performance
6. (LP)DDR4/5 spec: input timings
7. DDR3/4 spec: setup / hold derating
8. IDD current definition
9. Different DIMM types and physical implementation
10. Setup for flexible module density

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Agenda part 2

1. Error correction
2. Layout guidelines / DFT
3. Measurement and equipment
4. TDR measurement
5. Failure analysis
6. Transient simulation
7. PDN simulation
8. S-Parameters
9. Rules of thumb and some theory

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Agenda part 3

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1. Overview on training options
2. Power up sequence and “low speed signaling”
3. ZQ calibration
4. CA bus calibration (per CA bus or per bit)
5. Write leveling
6. Write DQS / DQ timing alignment (per byte or per bit)
7. Receive enable training via MPR
8. Read DQS / DQ timing alignment (per byte or per bit)
9. DDR4 VrefDQ training
10. Conclusion