Open the Black Box of Memory

Agenda

Open the Black Box of Memory
Overview

- Goal: Provide detailed view for design, layout and test engineers working with DRAM
- Duration: 2 to 3 days (dependent on seminar format)
  - To cover all information in the handout would take more time, so some topics are selected based on participant feedback
- The focus is on (LP)DDR4/5 based on the changes from previous generations. This allows an easy transition for engineers knowing DDR3 to DDR4/5 and LPDDR4/5 memory.
- Deep dive for many topics
  - On the fly specific topics that can be discussed more intensive
  - If a very close insight into some special features is required, please contact EyeKnowHow directly

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Agenda part 1

- Seminar target and overview
- Different applications and memories
- DRAM basics
- Evolution of commodity DRAM generations
- Memory system performance
- (LP)DDR4/5 spec: input timings
- DDR3/4 spec: setup / hold derating
- IDD current definition
- Different DIMM types and physical implementation
- Setup for flexible module density

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Agenda part 2

- Error correction
- Layout guidelines / DFT
- Measurement and equipment
- TDR measurement
- Failure analysis
- Transient simulation
- PDN simulation
- S-Parameters
- Rules of thumb and some theory

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Agenda part 3

- Overview on training options
- Power up sequence and “low speed signaling”
- ZQ calibration
- CA bus calibration (per CA bus or per bit)
- Write leveling
- Write DQS / DQ timing alignment (per Byte or per bit)
- Receive enable training via MPR
- Read DQS / DQ timing alignment (per Byte or per bit)
- DDR4 VrefDQ training
- DQS clock tree training
- Conclusion